UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER DECEMBER 2011

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ELECTRONICS III
COURSE CODE:	E511
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. **There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
2. **If you think not enough data has been given in any question you may assume any reasonable values.**

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

(a) A two stage IC amplifier is shown in Figure-Q1.

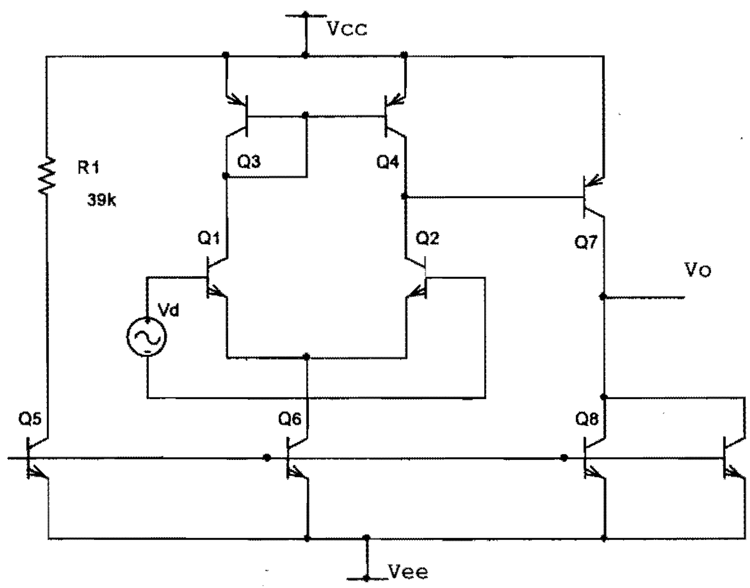

Figure-Q1

Assume that the input bias currents are drawn from the signal source. The two parallel transistors are represented by Q8 as a single equivalent. You may assume the following data.

For pnp: $V_A = 50V$ $\beta = 75$

For npn: $V_A = 120V$ $\beta = 100$

$V_{CC} = 10V$ $V_{EE} = -10V$

Find the following.

(a) Collector Currents of all transistors at no signal.

(3 marks)

(b) Differential input impedance.

(4 marks)

(c) Voltage gain $\frac{v_o}{v_d}$.

(15 marks)

(d) Output impedance.

(3 marks)

QUESTION TWO *(25 marks)*

A circuit of the Widlar current source is shown in Figure-Q2. Assume that the transistors are matched and the β is large unless otherwise stated.

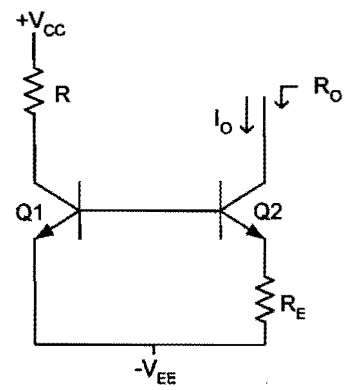

Figure-Q2

(a) Show that the current I_O is given by

$$I_O = \frac{V_T}{R_E} \ln\left[\frac{V_{CC} - V_{BE} + V_{EE}}{RI_O}\right].$$

(5 marks)

(b) Derive an expression for the output resistance R_O.

(10 marks)

(c) Design the current source for $I_O = 500\mu A$ with $\pm 10V$ supplies.

(5 marks)

(d) Assuming $\beta = 100$ and $V_A = 100V$,

(i) Find the minimum possible voltage at the output while maintaining proper operation of the current source.

(ii) Also calculate the output resistance.

(5 marks)

QUESTION THREE *(25 marks)*

A block diagram of an IC op-amp is shown in Figure-Q3.

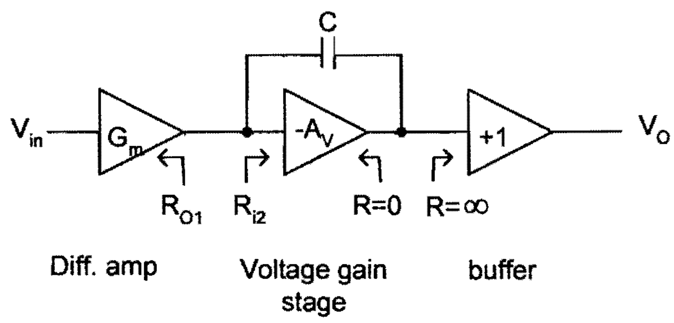

Figure-Q3

(a) It is required to introduce a dominant pole at $10Hz$ for frequency compensation. The impedances R_{O1} and R_{i2} are $2M$ and $1.5M$ respectively. If $A_V = 500$, find the value of the compensation capacitor C.

Note that the value of G_m is not given intentionally.

(7 marks)

(b) Assuming the DC gain of the op-amp is $100dB$,

(i) Find the unity gain bandwidth using the data given in (a).

(ii) If the amplifier is used with negative feedback and the feedback factor is 0.01, find the resulting bandwidth.

(10 marks)

(c) If the total bias current available in the differential amplifier stage is $20\mu A$, find the slew rate and the full power bandwidth. Assume that the maximum available output is $10V$.

(8 marks)

QUESTION FOUR (*25 marks*)

An integrated circuit CMOS amplifier is shown in Figure-Q4.

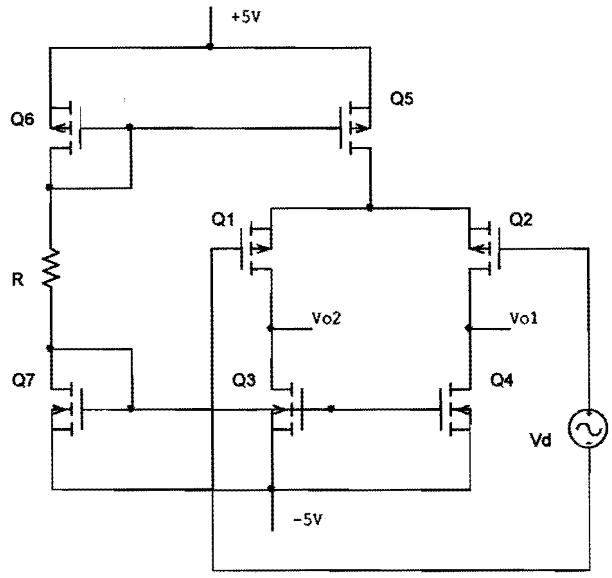

Figure-Q4

The voltage V_d is the input and the voltages V_{o1} and V_{o2} are the outputs. The sets of matching transistors are $[Q_6, Q_5]$, $[Q_1, Q_2]$, $[Q_3, Q_4]$. Some of the design data of the amplifier are given below.

Differential gain $\frac{V_{o1} - V_{o2}}{V_d} = -50$ Reference current $= 200\mu A$

Voltage at the gate of Q_6 $= 1.5V$ Voltage at the gate of Q_7 $= -1.5V$

Process parameters:

$V_A = 20V$ (for all transistors) $K'_p = 50\frac{\mu A}{V^2}$

$K'_n = 100\frac{\mu A}{V^2}$ $|V_t| = 2.5V$

(a) Find the bias currents of all transistors and the value of R.

(5 marks)

(b) Show that the differential gain $\left(\frac{V_{o1} - V_{o2}}{V_d}\right) = -V_A\sqrt{\frac{K_P}{I_{D2}}}$

(8 marks)

(c) Find the $\left(\frac{W}{L}\right)$ values of each transistor.

(12 marks)

QUESTION FIVE (25 *marks*)

(a) Demonstrate the translinear principle using a loop of four npn transistors. What are the factors which deviate its behavior from ideal conditions?

(7 marks)

(b) Analyze the circuit shown in Figure-Q5 using the translinear principle and find out the function represented by I_{out} .

(15 marks)

(c) Comment on the working range of the input signals.

(3 marks)

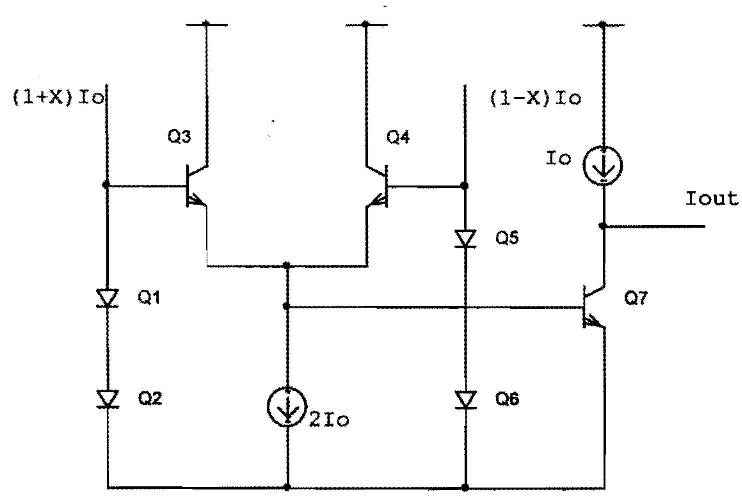

Figure-Q5

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

$$V_A = 1/\lambda$$

2. BJT EBERS-MOLL EQUATIONS

$$i_E = \frac{I_s}{\alpha_F}\left(e^{v_{BE}/V_T} - 1\right) - I_s\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_C = I_s\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \frac{I_s}{\beta_F}\left(e^{v_{BE}/V_T} - 1\right) + \frac{I_s}{\beta_R}\left(e^{v_{BC}/V_T} - 1\right)$$

3. Unless otherwise stated, $V_{BE(ON)} = 0.7$ V and $V_T = 0.025$ V.