UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS II

COURSE CODE – EE324

MAIN EXAMINATION

MAY 2012

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. There are FIVE questions in this paper. Answer any FOUR questions only.
2. Each question carries equal marks.
3. Show all your steps clearly in any calculations.
4. State clearly any assumptions made.
5. Start each new question on a fresh page.

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Question 1

(i) Explain the differences among:

a. *address lines* and *memory addresses*. [2]
b. A *Boolean equation*, a *state equation*, a *characteristic equation*, and a *flip-flop input* equation. [4]

(ii) A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

a. Tabulate the characteristic table. [2]
b. Tabulate the excitation table. [2]
c. Derive the characteristic equation. [3]
d. Show how the PN flip-flop can be converted to a D flip-flop. [4]

(iii) Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table of a binary multiplier that multiplies two 5-bit numbers. [3]

(iv) With the aid of diagram (or diagrams), explain how a Master-Slave D flip-flop works. Explain the rationale for having this type of circuit edge-triggered rather than level-triggered. [5]

Question 2

(a) A RAM chip of 8192x8 bits has two chip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw a block diagram and label all input and output terminals in the RAM. [5]

(b) Using a PLA, implement a combinational circuit that evaluates the quadratic equation:

$$x^2 + x + 15$$

WHERE:

x is a 4-bit binary number.

Use the minimum number of product terms in your implementation. [20]

Question 3

Derive the state table, state diagram, and Boolean expressions for the outputs O_0 to O_2 in the circuit diagram shown in Figure Q3. Explain the function the circuit performs. [25]

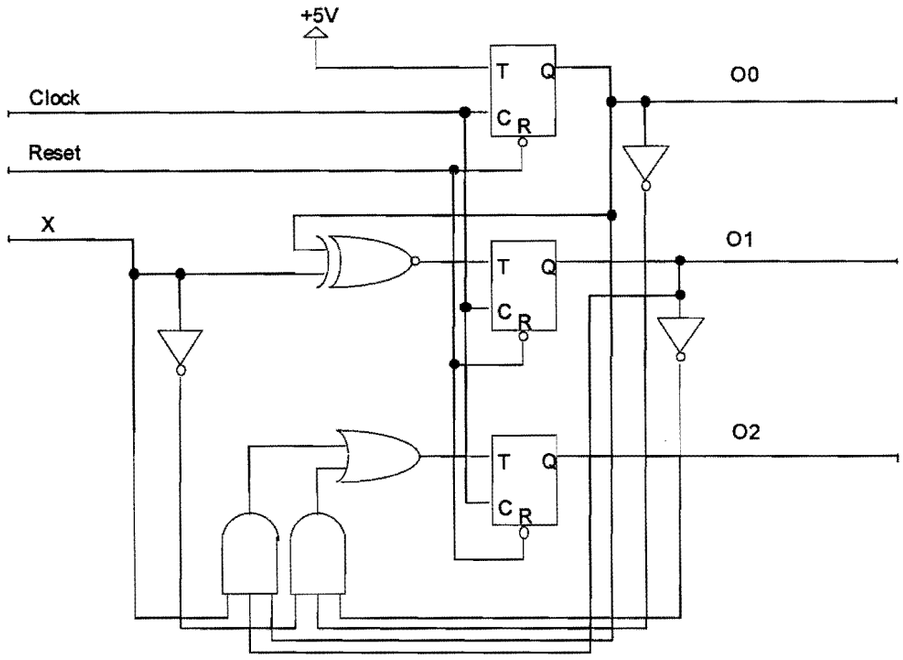

Figure Q3. Circuit diagram for Question 3

Question 4

Using only a shift register and a ROM of suitable sizes, design a *Mealey* sequential circuit that detects the sequence 01011. Explain how your design satisfies the behavioural requirements of the sequence detector. [25]

Question 5

(i) Design a timing circuit that provides an output signal that stays on for exactly eight clock cycles. A start signal sends the output to the 1 state, and after eight clock signals returns to the 0 state. [14]

(ii) Discuss the instruction execution cycle in a microprocessor. [6]

(iii) Using examples, compare and contrast Mealy and Moore models of Finite State Machines. [5]

END OF PAPER