UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER DECEMBER 2011

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. **There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
2. **If you think not enough data has been given in any question you may assume any reasonable values.**

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SIX (6) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

Consider the differential amplifier shown in Figure-Q1.

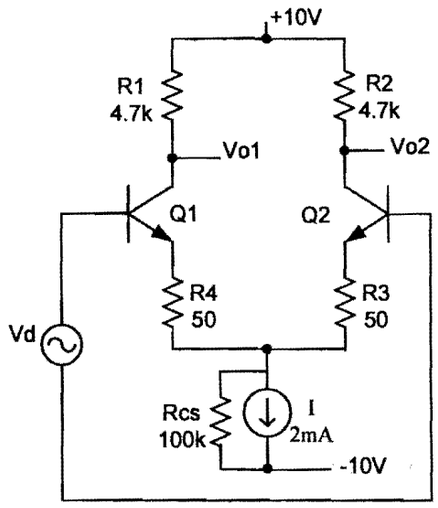

Figure-Q1

(a) Find the differential input resistance. Assume β = 100. (3 marks)

(b) Draw the differential half circuit. Hence calculate the voltage gains $\frac{V_{o2}}{V_d}$ and $\frac{V_{o2}-V_{o1}}{V_d}$. (7 marks)

(c) Draw the common mode half circuit. Then calculate the common mode gain at the output V_{o2} and CMRR in dB. (7 marks)

(d) Estimate the high frequency 3dB bandwidth if $R_4 = R_3 = 0$.

$C_\pi = 13pF$ $C_\mu = 2pF$ $r_o = \infty$ (8 marks)

QUESTION TWO *(25 marks)*

(a) For the circuit shown in Figure-Q2(a), the two transistors Q1 and Q2 are matched.

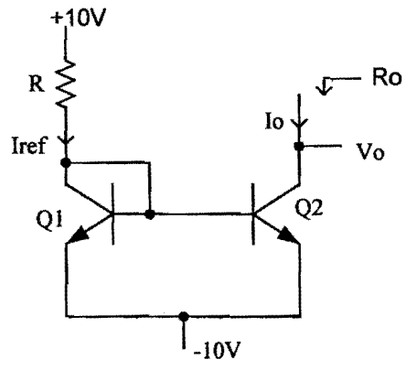

Figure-Q2(a)

(i) If the current gain of the transistors are β,

1.1 Find an expression for I_o with I_{ref}.

1.2 Calculate the value of R to have an $I_o = 1mA$. Assume $\beta = 75$.

(5 marks)

(ii) What is the output resistance R_o? Find the value of the output current I_o, if the output voltage V_o is 5V. Assume $V_A = 100V$. (9 marks)

(b) Consider the current source shown in Figure-Q2(b). You may assume that the transistors are matched.

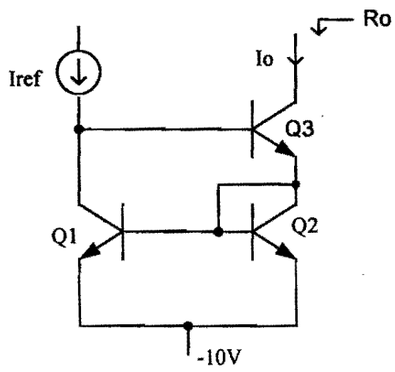

Figure-Q2(b)

(i) Derive the percentage change of I_o with respect to I_{ref}. (6 marks)

(ii) Calculate the value of R_o. You may use any formula known to you.

$I_{ref} = 100\mu A$ $V_A = 120V$ $\beta = 100$ (3 marks)

(iii) State two advantages of this circuit. (2 marks)

QUESTION THREE ***(25 marks)***

(a) A circuit of an enhancement type NMOS amplifier is shown in Figure-Q3(a).

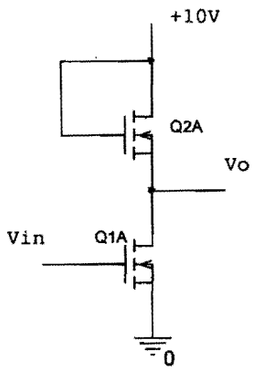

Figure-Q3(a)

For this amplifier, following process parameters are given.

$W_1 = 100\mu m$ $L_1 = 6\mu m$ $W_2 = 1\mu m$ $L_2 = 6\mu m$ $V_t = 1V$

(i) Obtain a relationship between V_o and V_{in} for dc voltages. Calculate V_o if $V_{in} = 1.5V$. (10 marks)

(ii) Draw the small signal equivalent circuit. Hence derive an expression for the voltage gain and calculate its value. (8 marks)

(b) For the CMOS amplifier shown in Figure-Q3(b),

$K_n = K_p = 100\mu A/V^2$ $V_{tn} = |V_{tp}| = 1V$ $V_{An} = V_{Ap} = 100V$ $I_{ref} = 100\mu A$.

Find the small signal voltage gain. (7 marks)

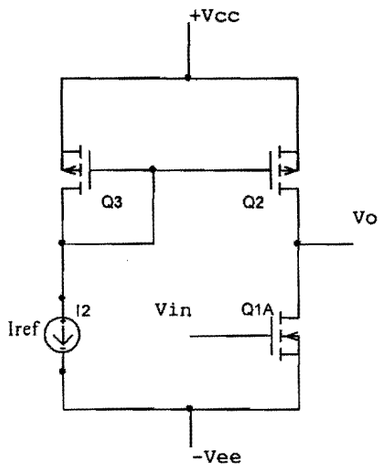

Figure-Q3(b)

QUESTION FOUR (*25 marks*)

Consider the cascode amplifier shown in Figure-Q4.

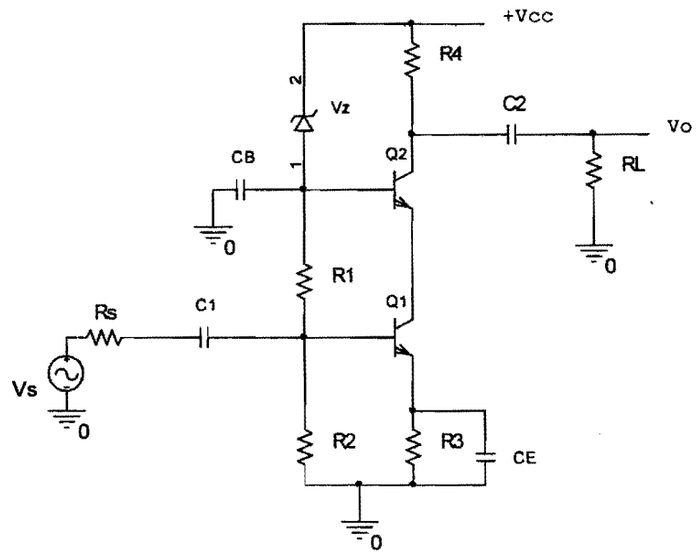

Figure-Q4

(a) Assuming that the transistors are identical,

(i) Find an expression for the mid band voltage gain.

(ii) Calculate the mid band gain for the data given below.

$R_S = 2k$ $R_1 = 5k$ $R_2 = 8k$ $R_3 = 1k$ $R_4 = 5k$ $R_L = 3k$ $Vz = 5V$

$\beta = 100$ $I_{C2} = 1mA$ (13 marks)

(b) Find the values of the pole frequencies and hence determine the high frequency 3dB bandwidth. (12 marks)

QUESTION FIVE (25 *marks*)

A dc regulator circuit is shown in Figure-Q5.

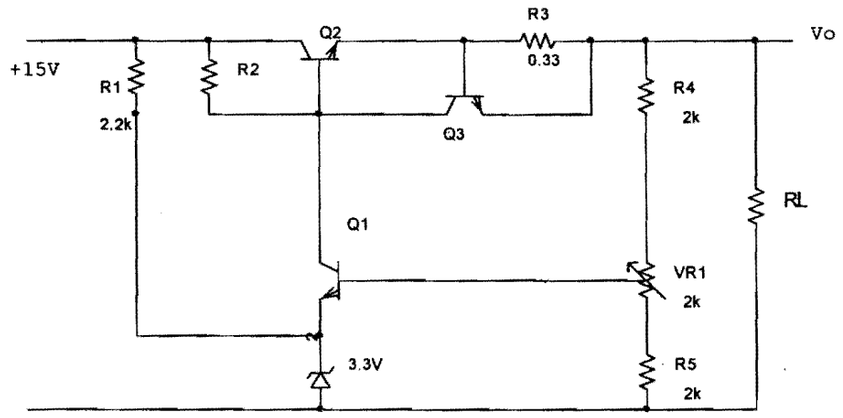

Figure-Q5

(a) Find the range of the output voltage V_o. (6 marks)

(b) Find an expression for the power dissipation in Q_2 in terms of the load current at a short circuit of the output.

(4 marks)

(c) Derive a relationship of the load current and the minimum load resistance that can be applied while maintaining the regulation.

(3 marks)

(d) If the minimum collector current of Q_1 is I_{C1L}, find an expression for R_2.

(6 marks)

(e) Calculate the maximum load current value. Then find out,

(i) The maximum power dissipation in Q_2.

(ii) The minimum load resistance.

(iii) The value of R_2. Assume that the $\beta = 20$ for Q_2 and $I_{C1L} = 5mA$.

(6 marks)

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

$$V_A = \frac{1}{\lambda}$$

2. Unless otherwise stated, $V_{BE(ON)} = 0.7V$ and $V_T = 0.025V$.