University of Swaziland
Faculty of Science and Engineering
Department of Electrical and Electronic Engineering

Main Examination 2012

Title of Paper: Analogue Design I

Course Number: EE321

Time Allowed: 3 hrs

Instructions:

1. Answer any four (4) questions.
2. Each question carries 25 marks.
3. Useful tables are attached at the end of the question paper

This paper should not be opened until permission has been given by the invigilator.

This paper contains six (6) pages including this page.

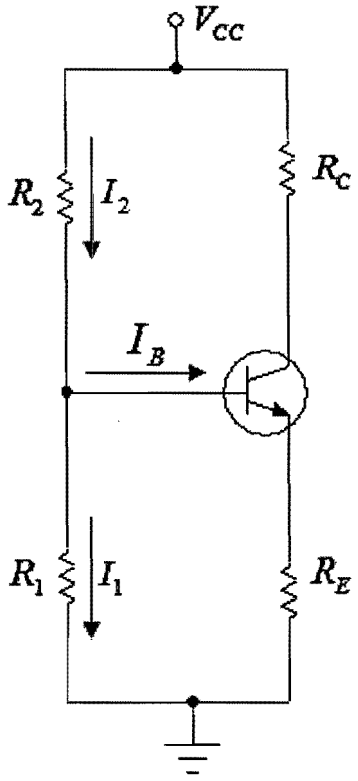
Question1

a) i) What is the main feature of the differential amplifier? [1]

ii) What do you understand by transistor biasing? [2]

b) What advantages does the voltage divider biasing have over the other biasing techniques? [2]

c) Design a voltage divider biased network to give $V_{CE} = 5V$ and $I_C = 750\mu V$. Take $\beta = 100$, $V_{BE} = 0.7V$, $V_{CC} = 15V$, $I_2 = 10I_B$, $I_1 = 9I_B$. Consider standard E12 range resistors for your final design. [20]



Question 2

a) Differentiate between the characteristics of a common-collector and common-base bipolar junction transistor (BJT) amplifier. [6]

b) A parallel resonant circuit has a capacitor of $100\,pF$ in one branch and inductance of $100\mu H$ plus a resistance of 10Ω in the parallel branch. If the supply voltage is $10V$, calculate:

i) The resonant frequency [3]
ii) The impedance of the circuit [3]
iii) The line current at resonance [3]
iv) The Q-factor of the circuit. [3]

c) Define what is meant by Common-Mode Rejection Ratio (CMRR). [2]

d) What is current gain-bandwidth product? [2]

e) Draw a simple circuit to show DC Bias with Voltage Feedback [3]

Question 3

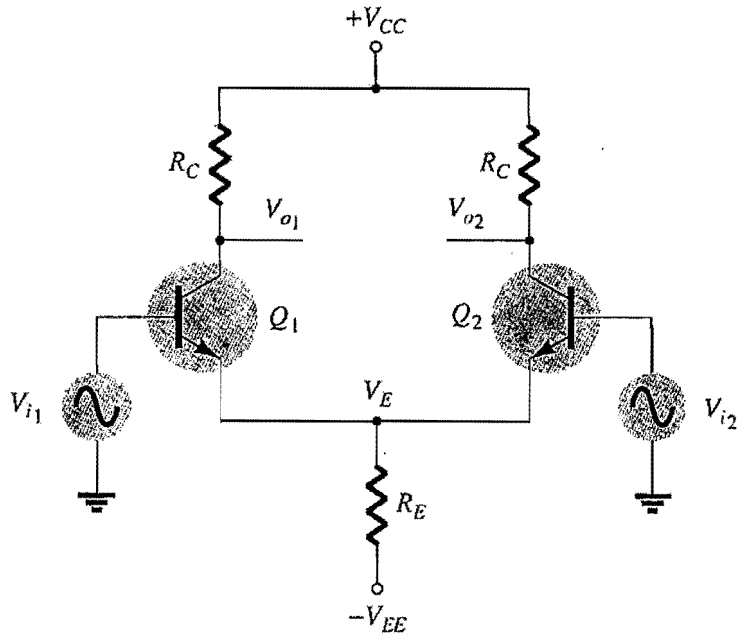
(a) Differentiate between an ideal and non-ideal op amp. [4]

(b) Draw any non-linear op amp amplifier circuit. [4]

(c) Determine the output voltage of an op amp for input voltages of $V_{i_1} = 150\mu V$ and $V_{i_2} = 140\mu V$. The amplifier has a differential gain of $A_d = 4000$ and the value of Common-Mode Rejection Ratio (CMRR):

(i) 100 [4]
(ii) 10^5 [4]

(d) Derive an expression for the voltage gain for the following circuit. Assume both transistors are well matched and R_E is very large. [5]



(e) Define op amp compensation. [2]

(f) Define slew rate. [2]

Question 4

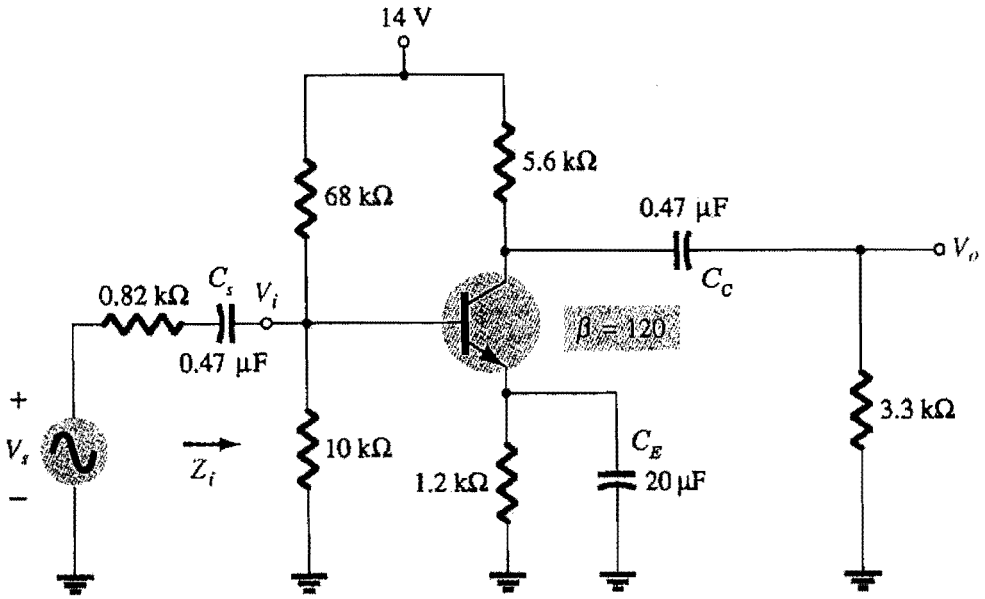
a) A certain amplifier has an input power of 1W and an output power of 100W. Calculate the dB power gain of the amplifier. [2]

b) For the network below, determine:

(i) f_{L_s}, low frequency response due to the input coupling capacitor C_s. [10]

(ii) f_{L_C}, the cut-off frequency due to output coupling capacitor C_C. [5]

with $V_T = 26mV$, $r_o = \infty\Omega$ and $V_{BE} = 0.7V$.

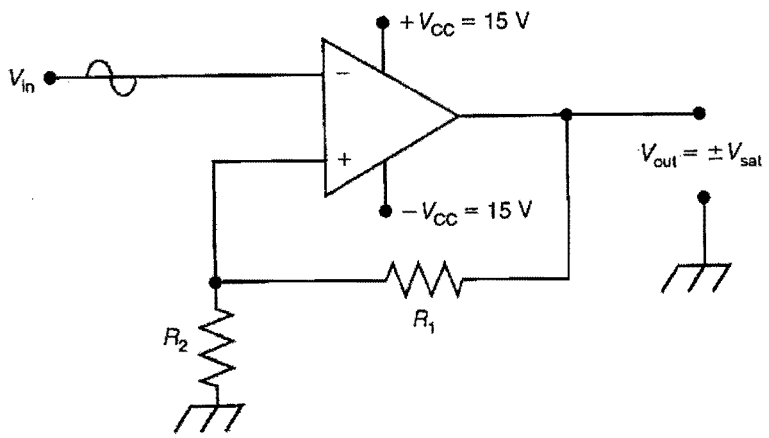


c) In the figure below, $V_{sat} = \pm 13V$, $R_1 = 1k\Omega$ and $R_2 = 100k\Omega$. Calculate:

i) The upper threshold point (UTP) [4]

ii) The lower threshold point LTP [2]

iii) The hysteresis voltage (V_H) [2]



Question 5

Consider the circuit below:

a) What circuit configuration is this, common-emitter or common-collector or common-base? [1]

b)

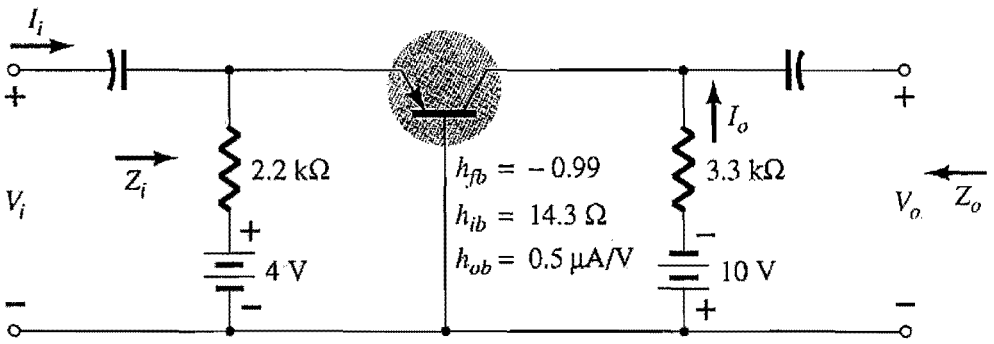
i) Draw the small signal hybrid model. [3]

ii) Calculate Z_i [3]

iii) Calculate Z_o [3]

iv) Calculate A_v [3]

v) Calculate A_i [2]



c) For the low pass filter below, with $C_F = 0.01\mu F$, $R_F = 10k\Omega$ and $R_i = 1k\Omega$. Calculate the voltage gain at $1MHz$. [10]