UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS I

COURSE CODE – EE322

MAIN EXAMINATION DECEMBER 2012

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

i. There are FIVE questions in this paper. Answer any FOUR questions only.

ii. Each question carries equal marks.

iii. Show all your steps clearly in any calculations.

iv. State clearly any assumptions made.

v. Start each new question on a fresh page.

DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Question 1

(a) Using the tabular method, minimize the following Boolean function:

$$F(A, B, C, D) = \sum(1, 3, 4, 5, 10, 11, 12, 13, 14, 15) \quad [12]$$

(b) Simplify the following using a k-map:

(i) $F = abc + cd + a'd + a'b$ [5]

(ii) $F(A,B,C,D) = \sum(1, 3, 5, 7, 9, 15)$ [4]
$d(A, B, C, D) = \sum(4, 6, 12, 13)$

(c) Using Boolean algebra simplify the following Boolean expression to a minimum number of literals:

$$F = (x'y' + z)' + z + xy + wz \quad [4]$$

Question 2

Analyse the combinational circuit shown in Figure Q2 and determine the following:

(a) Truth table. [12]
(b) Boolean function of the output F. [5]
(c) Timing Diagram showing how change in input relates to change in output with time. [8]

Show all working.

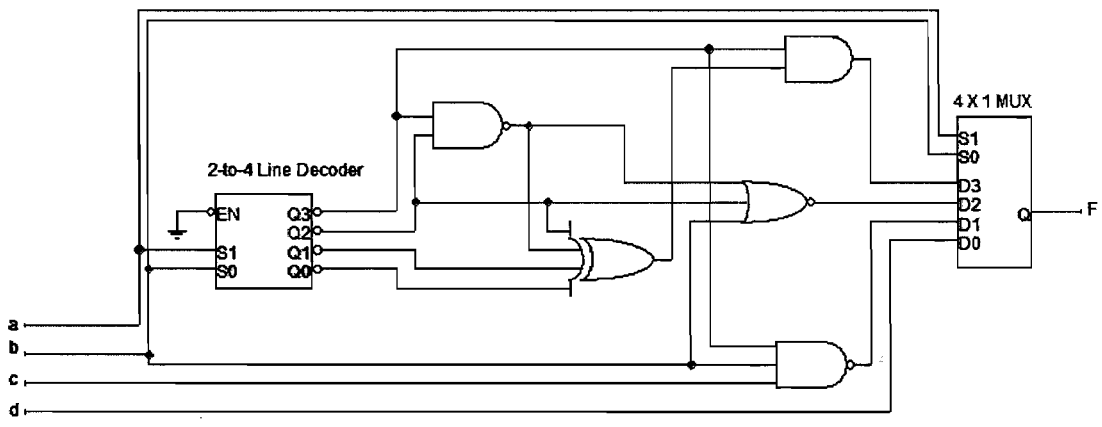

Figure Q2: Diagram for question 2

Question 3

(a) Derive the Boolean expressions for the output sum and output carry in a full adder circuit with inputs x_i, y_i, and c_i.

[6]

(b) Assuming that the *carry propagate* and *carry generate* are defined as

$$P_i = x_i + y_i$$
$$G_i = x_i y_i$$

respectively, show that the output carry and output sum of a full adder becomes

$$C_{i+1} = (C'_i G'_i + P'_i)' \quad [8]$$
$$S_i = (P_i G'_i) \oplus C_i \quad [7]$$

(c) Design a half-subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x – y and places the difference in D and the borrow in B.

[4]

Question 4

Figure 4 shows two devices *A* and *B*, which communicate through *Interface I*. Device B takes as input a 3-bit binary number in the range 0_{10}-5_{10} and outputs a binary number equivalent to the input binary number multiplied by 3. Device B sends its output to Device A. However, Device A only understands information presented in the hexadecimal numbering system. On the one hand, Device B only outputs information presented in the binary numbering system.

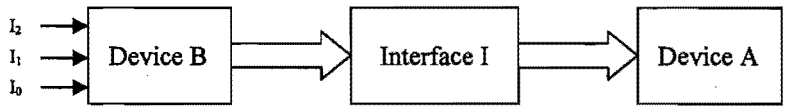

Figure 4: Diagram for question 4

Design two combinational circuits:

(a) A circuit for Device B, which ensures that the binary input $I_2I_1I_0$ is multiplied by 3.

(b) A circuit for Interface I, which ensures that data flowing from B to A is interpreted correctly at A. Use only one hexadecimal digit in Device A.

[25]

Question 5

(a) Using a minimum number of logic gates, design a combinational logic circuit which implements the following mathematical function:

```
f(x,y) = 3x + y
```

WHERE

```
x and y are 2-bit binary numbers.
```

[16]

(b) Implement the following Boolean function with a 4 x 1 multiplexer and external gates. [5]

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

(c) An 8 x 1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1, and S_0, respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Determine the Boolean function that the multiplexer implements. Express this Boolean function in sum-of-products form.

[4]

END OF PAPER