

**UNIVERSITY OF SWAZILAND  
MAIN EXAMINATION, FIRST SEMESTER DECEMBER 2012**

**FACULTY OF SCIENCE**

**DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING**

**TITLE OF PAPER: ANALOGUE DESIGN III  
COURSE CODE: EE421**

**TIME ALLOWED: THREE HOURS**

**INSTRUCTIONS:**

- 1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.**
- 2. If you think not enough data has been given in any question you may assume any reasonable values.**

**THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR**

**THIS PAPER CONTAINS EIGHT (8) PAGES INCLUDING THIS PAGE**

**QUESTION ONE (25 marks)**

A differential amplifier implemented with MOS devices is shown in Figure-Q1.

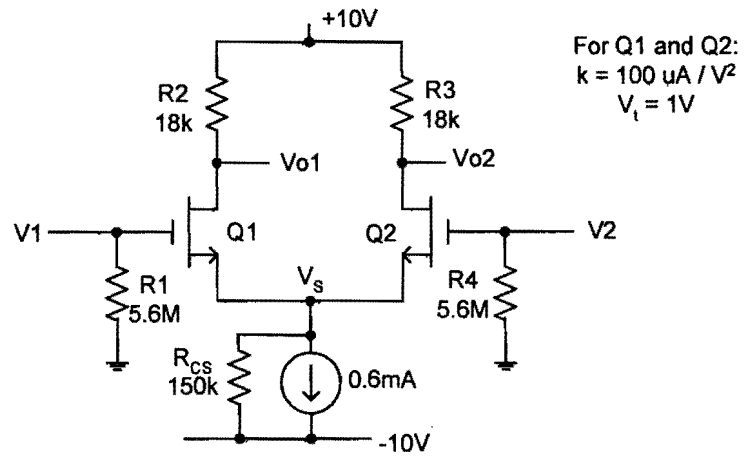


Figure-Q1

- (a) Calculate the transconductance  $g_m$  of the devices under the shown operating conditions. (4 marks)
- (b) If  $V_1 = 100\text{mV}$  and  $V_2 = -100\text{mV}$ , calculate the drain currents and drain voltages of the transistors. (5 marks)
- (c) A differential signal  $v_d$  is applied to the inputs (ie,  $v_d = v_1 - v_2$ ).
- Draw the differential half circuit for ac signals.
  - Calculate the voltage gains  $\frac{v_{o2}}{v_d}$  and  $\frac{v_{o2} - v_{o1}}{v_d}$ .

(8 marks)

- (d) If a common mode signal  $v_{cm}$  is applied to the inputs,

- Draw the common mode half circuit for the ac signals and find the common mode gain at the output  $v_{o2}$ .
- Calculate CMRR in dB.

(8 marks)

**QUESTION TWO (25 marks)**

- (a) A circuit of a BJT current source is shown in Figure-Q2(a). You may assume that the transistors are matched.

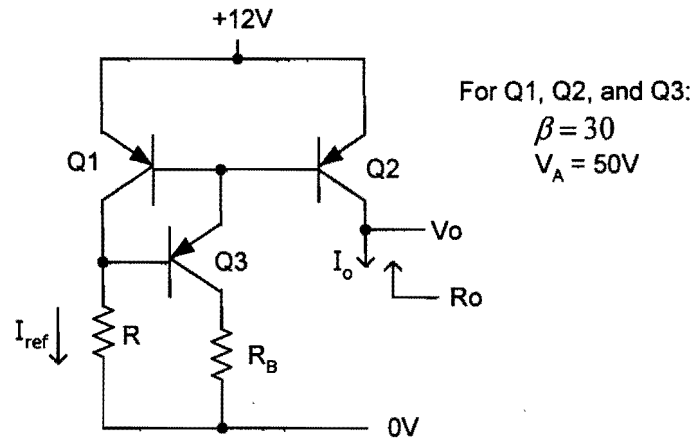


Figure-Q2(a)

- (i) Find an expression for the current  $I_o$  in terms of  $I_{ref}$  and  $\beta$ , where  $\beta$  is the current gain of the transistors. (5 marks)
- (ii) Find suitable values for  $R$  and  $R_B$  to have  $I_o = 1mA$ . (4 marks)
- (iii) Find the output resistance  $R_o$ . If  $V_o = 5V$ , what is the output current  $I_o$ ? (5 marks)
- (b) A current mirror implemented with NMOS transistors in an integrated circuit is shown in Figure-Q2(b).

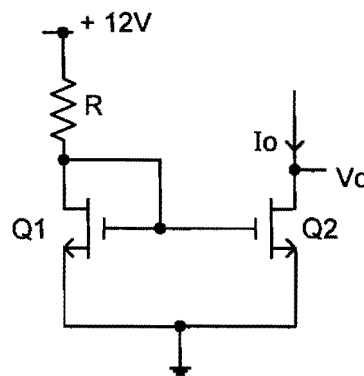


Figure-Q2 (b)

Following are the some of device parameters for Q1 and Q2.

$$L_1 = L_2 = 10\mu m \quad W_1 = 30\mu m \quad W_2 = 60\mu m \quad V_t = 1V \quad \mu C_{ox} = 50 \frac{\mu A}{V^2}$$

The output current  $I_o = 100\mu A$ .

- (i) What is the value of  $V_{GS}$ ? (3 marks)
- (ii) Calculate the value of  $R$ . (3 marks)
- (iii) When  $V_o$  is raised to 8 volts,  $I_o$  becomes  $110\mu A$ . Estimate the output resistance of the mirror and the Early voltage of the devices. (5 marks)

**QUESTION THREE (25 marks)**

- (a) In the circuit shown in Figure-Q3(a), the transistors  $Q_1$  and  $Q_2$  are matched and of high gain type. For all transistors,  $V_A = 100V$  and for  $Q_3$ ,  $\beta = 100$ .

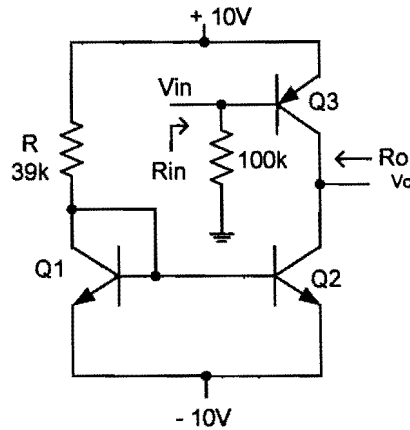


Figure - Q3(a)

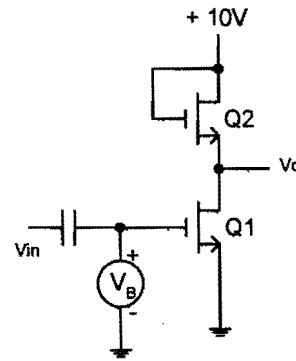


Figure-Q3 (b)

- (i) Calculate the collector current of  $Q_3$  at no signal. (3 marks)
- (ii) Derive an expression for the voltage gain  $\left(\frac{v_o}{v_{in}}\right)$  and find its value. (4 marks)
- (iii) Find the input and output impedance of the circuit. (4 marks)

- (b) An enhancement type NMOS amplifier is shown in Figure-Q3(b). You may use the following device parameters.

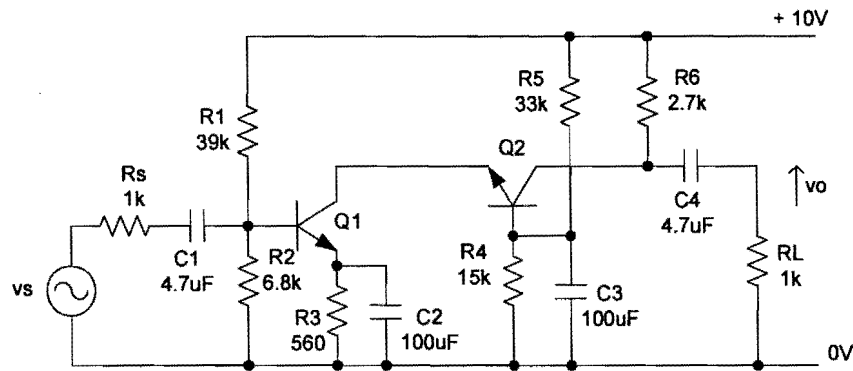
$$W_1 = 150\mu m \quad W_2 = 10\mu m \quad V_t = 2V \quad \mu C_{ox} = 100 \frac{\mu A}{V^2}$$

$$L_1 = 10\mu m \quad L_2 = 50\mu m$$

- (i) Calculate the bias voltage  $V_B$  required to keep  $V_o = 5V$  at no signal. (6 marks)
- (ii) Draw the small signal equivalent circuit. Hence derive the voltage gain  $\frac{v_o}{v_{in}}$  and find its value. (8 marks)

**QUESTION FOUR (25 marks)**

(a) A circuit of a cascode amplifier is shown in Figure-Q4.



**Figure - Q4**

Assume that the transistors are of high gain type.

- (i) Show that the collector currents of the transistors are 1.58mA. Hence calculate the collector voltages under quiescent conditions.

(6 marks)

- (ii) Derive an expression for the mid-band gain and calculate its value. Assume that the  $\beta = 100$  and  $I_{c1} = I_{c2} = 1.58mA$ .

(8 marks)

- (iii) Find the values of the three pole frequencies and hence determine the high frequency 3dB bandwidth.

$$C_{\pi} = 15pF \quad C_{\mu} = 3pF$$

(11 marks)

**QUESTION FIVE (25 marks)**

A dc voltage regulator circuit is shown in Figure-Q5.

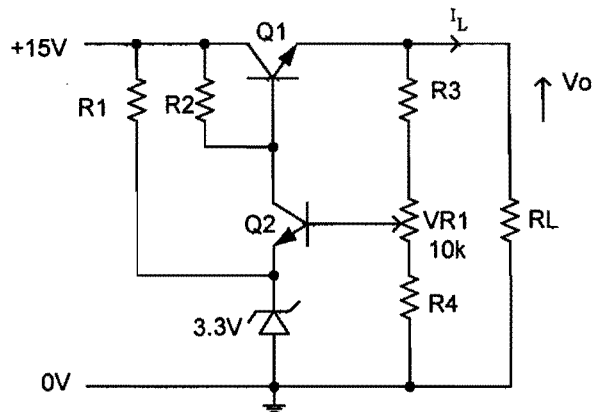


Figure-Q5

- (i) Calculate the values of  $R_3$  and  $R_4$  in order to have maximum and minimum output voltages of 12V and 4V respectively. (6 marks)
- (ii) If the maximum load current  $I_L = 1.5A$ , find the maximum power dissipation requirement of  $Q_1$ . (4 marks)
- (iii) Show the implementation of an active current limit protection for  $Q_1$  and find the related component values with power rating. (5 marks)
- (iv) Assuming a minimum collector current of 5mA for  $Q_2$ , find the value of  $R_2$  and its power rating. The  $\beta$  of  $Q_1 = 25$ . (5 marks)
- (v) What is the power rating of the zener diode? If the zener diode requires a minimum current of 10mA, find the value of  $R_1$ . (5 marks)

## USEFUL FORMULAE:

$$I_D = \frac{I}{2} \pm \sqrt{2KI} \left( \frac{v_{id}}{2} \right) \sqrt{1 - \frac{\left( \frac{v_{id}^2}{4} \right)}{I/2k}}$$