UNIVERSITY OF SWAZILAND

SUPPLIMENTERY EXAMINATION, SECOND SEMESTER

JULY 2013

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

A differential amplifier circuit is shown in Figure-Q1. Assume that the $V_{BE} = 0.6V$ and the transistors are matched with $\beta = 100$.

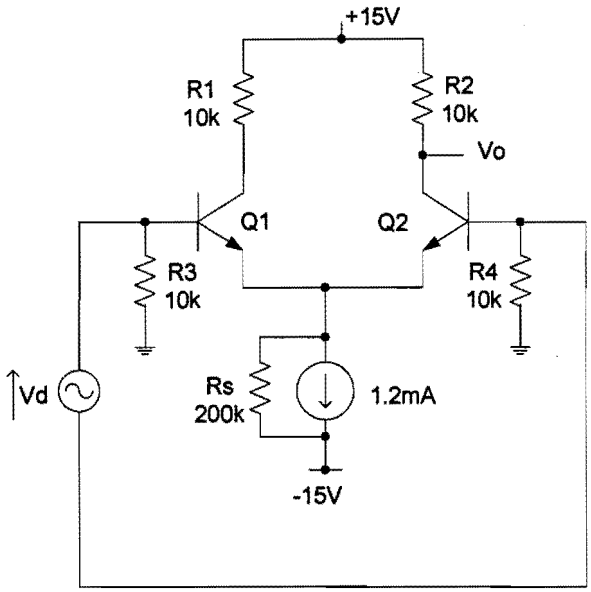

Figure-Q1

(a) Find the following under the quiescent conditions.

(i) Collector voltage of Q_2.

(ii) Base voltage of Q_1 and Q_2.

(6 marks)

(b) Draw the differential half circuit for ac signals and calculate the differential voltage gain $\frac{v_o}{v_d}$ deriving any formula you use.

(7 marks)

(c) Draw the common mode half circuit for ac signals and find the common mode gain at the output v_o. Hence calculate the CMRR in dB. Derive any formula you use.

(7 marks)

(d) Find the differential input resistance and the differential output resistance.

(5 marks)

QUESTION TWO *(25 marks)*

(a) A Widlar current source is shown in Figure-Q2(a). The transistors Q_1 and Q_2 are matched and of high gain type.

(i) Find a relationship between I_o, R, R_S and V_{CC}.

(6 marks)

(ii) Design this current source for $I_o = 150\mu A$, if the $V_{CC} = 12V$. Assume that for the transistors, when the $V_{BE} = 0.6V$, the $I_C = 0.76mA$.

(5 marks)

(iii) What is the output resistance R_o, if the $V_A = 100V$ and the $\beta = 100$?

(2 marks)

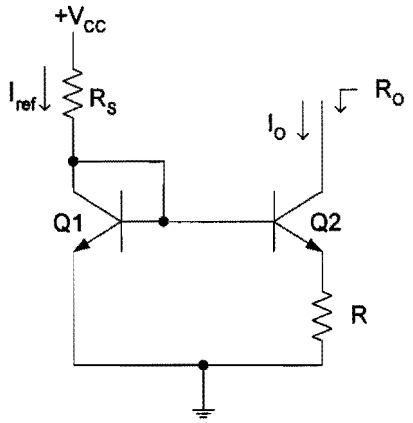

Figure-Q2(a)

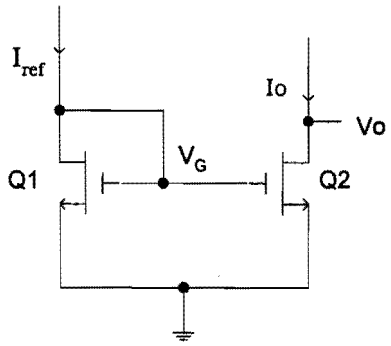

Figure-Q2(b)

(b) Consider the current mirror shown in Figure-Q2(b). Some of the process parameters of the devices are given below.

$L_1 = L_2 = 5\mu m$ $W_1 = 20\mu m$ $W_2 = 60\mu m$ $V_t = 2V$

$\mu C_{ox} = 50\frac{\mu A}{V^2}$ $V_A = 75V$

(i) Find the value of V_G for an output current of $I_o = 200\mu A$.

(4 marks)

(ii) Calculate the value of I_{ref}, when the $I_o = 200\mu A$.

(4 marks)

(iii) When $V_o = 10V$, estimate the output current I_o for the value of I_{ref} in (ii) above.

(4 marks)

QUESTION THREE *(25 marks)*

A circuit of a cascode BJT amplifier is shown in Figure-Q3.

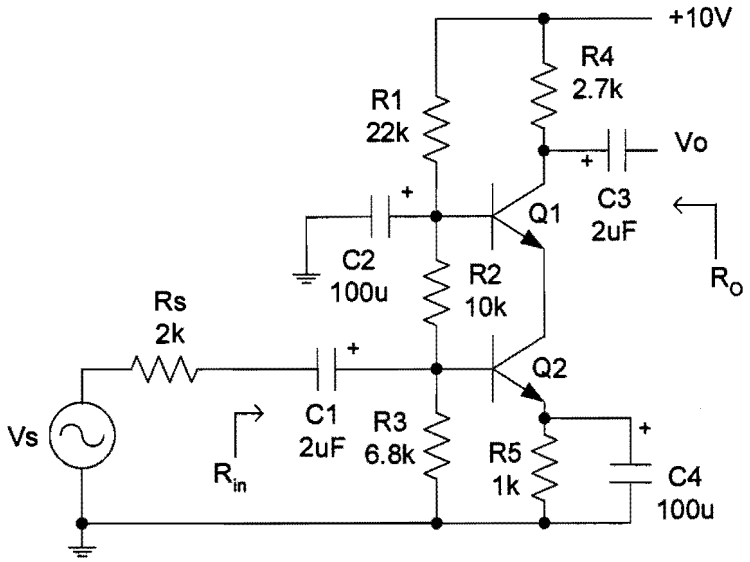

Figure-Q3

(i) Show that the collector current of Q_1 is $1.15mA$. Hence find the collector current and emitter voltage of each transistor at the quiescent conditions, assuming that the transistors are of high gain.

(10 marks)

(ii) Find an expression for the mid-band gain $\frac{v_o}{v_s}$, and calculate its value. Neglect the effect of r_o and assume that the $\beta = 100$.

(10 marks)

(iii) Estimate the values of R_{in} and R_o.

(5 marks)

QUESTION FOUR (*25 marks*)

(a) An IC amplifier is shown in Figure-Q4(a). Assume that the transistors are of high gain and matched.
Assuming that the $V_A = 100V$, $\beta = 100$ and $V_{BE} = 0.6V$ for all transistors, find

(i) the collector current of Q_3.

(2 marks)

(ii) an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value.

(7 marks)

(iii) the input impedance R_{in} and the output impedance R_o.

(4 marks)

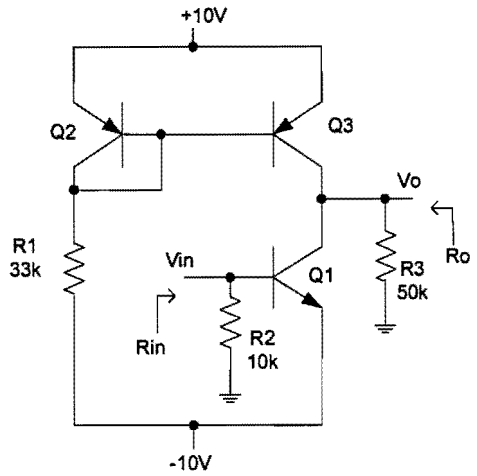

Figure-Q4(a)

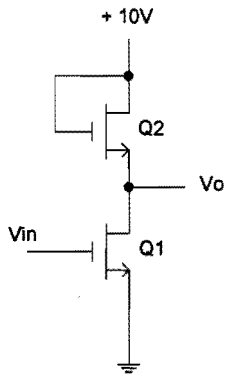

Figure-Q4(b)

(b) A circuit of an enhancement type NMOS amplifier is shown in Figure-Q4(b). Some useful parameters of the devices used in the circuit, are shown below.

$W_1 = 100\mu m$ $W_2 = 10\mu m$ $V_t = 1V$ $\mu C_{OX} = 150\frac{\mu A}{V^2}$
$L_1 = 10\mu m$ $L_2 = 40\mu m$

(i) Find the drain current of Q_2 when a dc voltage of $1.5V$ is applied to v_{in}. What is the value of v_o in this case?

(4 marks)

(ii) Draw the small signal equivalent circuit. Then derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value.

(8 marks)

QUESTION FIVE (25 *marks*)

Consider the voltage regulator circuit shown in Figure-Q5.

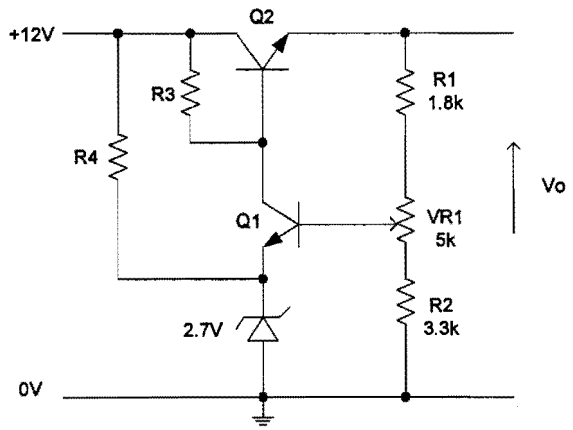

Figure-Q5

You may assume that the $V_{BE} = 0.6V$.

(i) Find the minimum and maximum output voltage.

(6 marks)

(ii) Find the maximum power dissipation of Q_2 if the maximum load current is $2A$.

(4 marks)

(iii) Draw the circuit of an active current limit for this regulator. Find the values and the power ratings of the resistor(s) used in your current limit circuit. Assume a maximum load current of 2A.

(5 marks)

(iv) Find the values of R_3 and R_4 using the following data.

$\beta_{Q2} = 20$ min. collector current of $Q_1 = 6mA$

Min. zener current = $5mA$ max. load current = $2A$

(5 marks)

(v) Determine the maximum power dissipation of R_3, R_4 and the zener diode.

(5 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.