

UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE & ENGINEERING
DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING
MICROCONTROLLERS AND MICROCOMPUTER SYSTEMS

COURSE CODE – EE423

MAIN EXAMINATION

MAY 2013

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. There are FIVE questions in this paper. Answer any FOUR questions only.
2. Each question carries equal marks.
3. Show all your steps clearly in any calculations.
4. State clearly any assumptions made.
5. Start each new question on a fresh page.

DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Question 1

- a) Discuss the instruction execution cycle in a microprocessor. [6]
- b) Fig. Q1.1 below shows the basic architecture of a microcontroller. Explain in detail the function of each of the following modules: CPU, Watch Dog Timer, and ADC. [7]

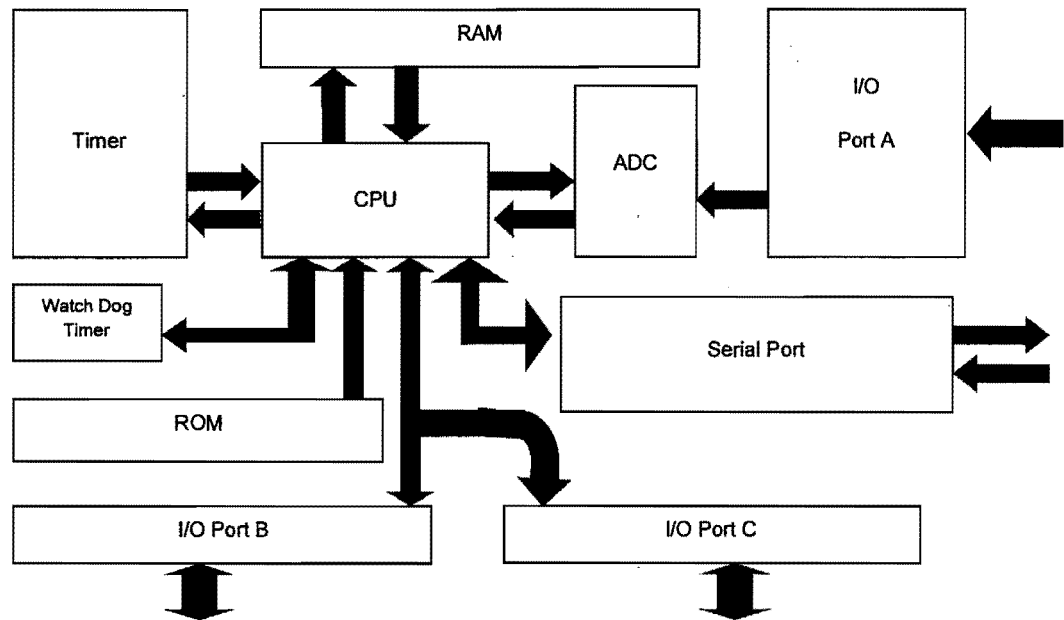


Figure Q1.1. Basic architecture of a microcontroller

- c) With the aid of appropriate illustrations, explain the Von Neuman and the Harvard architectures. Which architecture is used in PIC microcontrollers? [3]
- d) Explain the differences between the three groups/types of instructions available on PIC16F84 and PIC16F877 microcontroller instruction sets. [9]

Question 2

- (a) Discuss common addressing modes used in microprocessors. [9]
- (b) Identify and explain control unit architectures. [4]
- (c) Identify and explain the main components of the CPU. [5]
- (d) Write the assembly code for PIC16F84A (instruction set in Figure A1.0 of Appendix) based on the following operations. [6]
- Step 1: Set the origin to 0.
 - Step 2: Set the register R2 with hex data B8.
 - Step 2: Load the accumulator with decimal data 78
 - Step 3: Add 2 to R2
 - Step 4: If the accumulator is not equal to zero, decrease the accumulator value by 1
 - Step 5: Repeat Step 3 and Step 4 if the accumulator is not equal to zero

Question 3

Design a simple vending machine control system which uses the PIC16F84. The pin block diagram and instruction set are shown in Figures Q3.1 and A1.0 in the Appendix, respectively. The machine has the following properties:

- Accepts only E1 and E2 coins.
- Delivers a can of soft drink costing E3
- Provides change where appropriate.

Make the following assumptions in your design:

- The vending machine accepts 1 coin at a time through a coin recognizing interface which inputs an appropriate code to the system as follows: 00=no coin, 01=E1, and 10=E2.
- Generates a pulse of E1 or E2 when a coin is inserted.

The solution should be limited to the following:

- Draw a labelled block diagram showing which pins of the PIC will be used for inputs and outputs. [3]
- An FSM chart showing the operation of the vending machine. [8]
- An assembly language program for the vending machine controller. [14]

State any assumptions made.

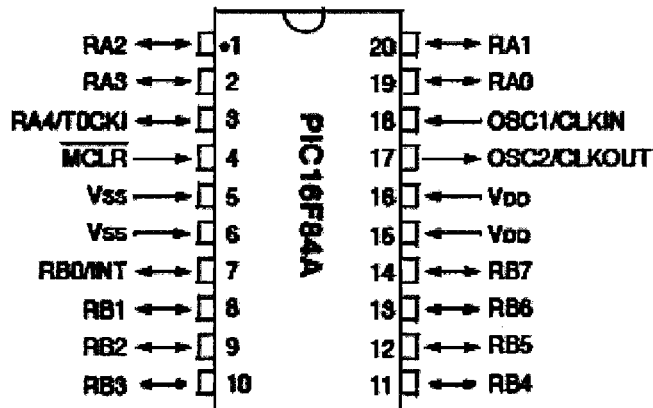


Fig. Q3.1 – Pin Diagram of PIC16F84A

Question 4

The block diagram of the PIC16F877 analogue to digital converter (ADC) is shown in Fig. Q4.1, and the ADCON0 register which controls it in Fig. Q4.2.

- What is the setting of the ADCON0 register if an external voltage reference is required, input channel 2 is selected, with clock source being FOSC divided by 2, and the ADC is switched on but not running? [6]

- (b) Why are different clock sources available for use with the ADC? [6]
- (c) What are the relative advantages in using an external or an internal (VDD) reference? [2]
- (d) When using the ADC, what are the main phases of operation which need to be considered? Describe any precautions which need to be taken, and any timing considerations. [11]

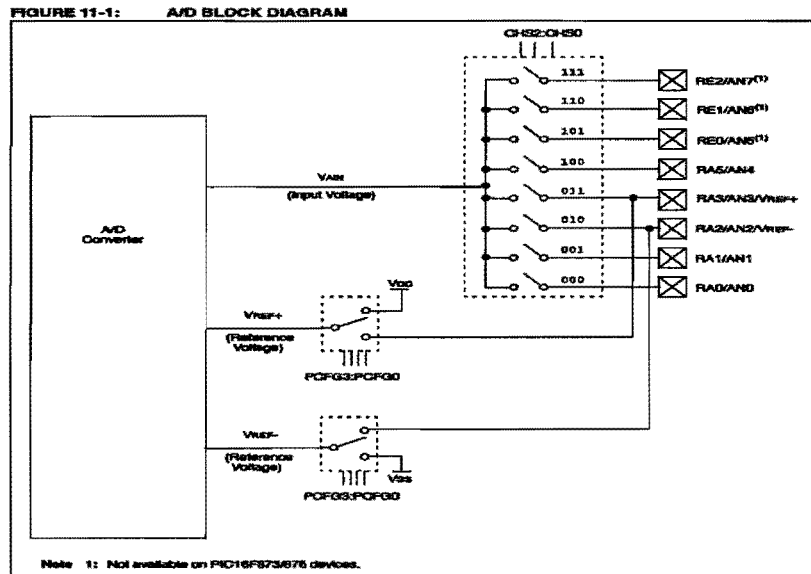


Fig. Q4.2 – Block Diagram of PIC16F877 Analogue to Digital Converter

REGISTER 11-1: ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE		ADON
bit 7							bit 0

- bit 7-6 **ADCS1:ADCS0: A/D Conversion Clock Select bits**
 00 = $F_{osc}/2$
 01 = $F_{osc}/8$
 10 = $F_{osc}/32$
 11 = FRC (clock derived from the internal A/D module RC oscillator)
- bit 5-3 **CHS2:CHS0: Analog Channel Select bits**
 000 = channel 0, (RA0/AN0)
 001 = channel 1, (RA1/AN1)
 010 = channel 2, (RA2/AN2)
 011 = channel 3, (RA3/AN3)
 100 = channel 4, (RA5/AN4)
 101 = channel 5, (RE0/AN5)⁽¹⁾
 110 = channel 6, (RE1/AN6)⁽¹⁾
 111 = channel 7, (RE2/AN7)⁽¹⁾
- bit 2 **GO/DONE: A/D Conversion Status bit**
 If ADON = 1:
 1 = A/D conversion in progress (setting this bit starts the A/D conversion)
 0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)
- bit 1 **Unimplemented: Read as '0'**
- bit 0 **ADON: A/D On bit**
 1 = A/D converter module is operating
 0 = A/D converter module is shut-off and consumes no operating current

Note 1: These channels are not available on PIC16F873/876 devices.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Fig. Q4.2 – PIC16F877 ADCON0 Register

Question 5

(i) A machine counts envelopes which are being packaged in packs of 150. The machine is controlled by a PIC 16F84. A sensor connected to the RA4/T0CK1 pin produces a logic pulse every time an envelope passes it. A block diagram of the Timer 0 module is shown in Fig. Q5.1, and the Option register in Fig Q5.2.

- Describe how you would configure the TMR0 to count the envelopes. Indicate what value you would set in the Option register. [8]
- Explain what strategy could be used to allow the microcontroller program to detect when the number 150 had been reached. [7]

(ii) In another application also using the 16F84, a regular timed interrupt is required. The clock oscillator frequency is 4MHz, and an interrupt frequency in the region of every 2ms is required. Describe how you would now configure the TMR0 module. [10]

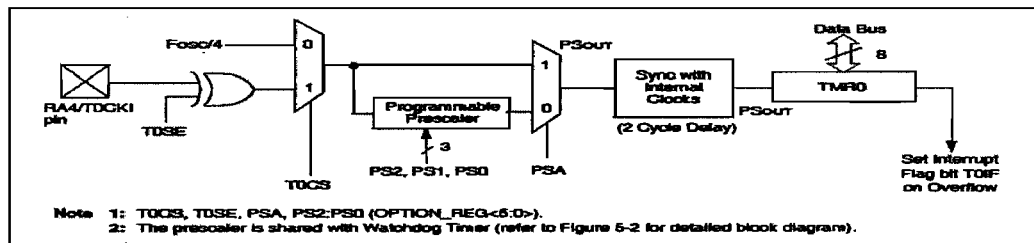


Fig. Q5.1 – The PIC16F84 TMR0 Module

2.3.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA=1), TMR0 has a 1:1 prescaler assignment.

REGISTER 2-2: OPTION REGISTER (ADDRESS 81h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBPUP	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7								
bit 7	RBPUP: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values							
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RBD/INT pin 0 = Interrupt on falling edge of RBD/INT pin							
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CK1 pin 0 = Internal Instruction cycle clock (CLKOUT)							
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CK1 pin 0 = Increment on low-to-high transition on RA4/T0CK1 pin							
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module							
bit 2-0	PS2:PS0: Prescaler Rate Select bits							
	Bit Value	TMR0 Rate	WDT Rate					
	000	1:2	1:1					
	001	1:4	1:2					
	010	1:8	1:4					
	011	1:16	1:8					
	100	1:32	1:16					
	101	1:64	1:32					
	110	1:128	1:64					
	111	1:256	1:128					

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Fig. Q5.2 – The PIC16F84 Option Register

Appendix

TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d Add W and f	1	00	0111 dfff ffff	G,DC,Z	1,2
ANDWF	f, d AND W with f	1	00	0101 dfff ffff	Z	1,2
CLRF	f Clear f	1	00	0001 lfff ffff	Z	2
CLRWF	- Clear W	1	00	0001 0xxx xxxx	Z	
COMF	f, d Complement f	1	00	1001 dfff ffff	Z	1,2
DECf	f, d Decrement f	1	00	0011 dfff ffff	Z	1,2
DECFSZ	f, d Decrement f, Skip if 0	1 (2)	00	1011 dfff ffff		1,2,3
INCf	f, d Increment f	1	00	1010 dfff ffff	Z	1,2
INCF	f, d Increment f, Skip if 0	1 (2)	00	1111 dfff ffff		1,2,3
IORWF	f, d Inclusive OR W with f	1	00	0100 dfff ffff	Z	1,2
MOVF	f, d Move f	1	00	1000 dfff ffff	Z	1,2
MOVWF	f Move W to f	1	00	0000 lfff ffff		
NOF	- No Operation	1	00	0000 0xxx0 0000		
RLF	f, d Rotate Left f through Carry	1	00	1101 dfff ffff	C	1,2
RRF	f, d Rotate Right f through Carry	1	00	1100 dfff ffff	C	1,2
SUBWF	f, d Subtract W from f	1	00	0010 dfff ffff	G,DC,Z	1,2
SWAPF	f, d Swap nibbles in f	1	00	1110 dfff ffff		1,2
XORWF	f, d Exclusive OR W with f	1	00	0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b Bit Clear f	1	01	00bb bfff ffff		1,2
BSF	f, b Bit Set f	1	01	01bb bfff ffff		1,2
BTFSQ	f, b Bit Test f, Skip if Clear	1 (2)	01	10bb bfff ffff		3
BTFS	f, b Bit Test f, Skip if Set	1 (2)	01	11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k Add literal and W	1	11	111x kkkk kkkk	C,DC,Z	
ANDLW	k AND literal with W	1	11	1001 kkkk kkkk	Z	
CALL	k Call subroutine	2	10	0kkk kkkk kkkk		
CLRWDI	- Clear Watchdog Timer	1	00	0000 0110 0100	TO,PD	
GOTO	k Go to address	2	10	1kkk kkkk kkkk		
IORLW	k Inclusive OR literal with W	1	11	1000 kkkk kkkk	Z	
MOVLW	k Move literal to W	1	11	00xx kkkk kkkk		
RETFIE	- Return from interrupt	2	00	0000 0000 1001		
RETLW	k Return with literal in W	2	11	01xx kkkk kkkk		
RETURN	- Return from Subroutine	2	00	0000 0000 1000		
SLEEP	- Go into standby mode	1	00	0000 0110 0011	TO,PD	
SUBLW	k Subtract W from literal	1	11	110x kkkk kkkk	G,DC,Z	
XORLW	k Exclusive OR literal with W	1	11	1010 kkkk kkkk	Z	

- Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

(00) Additional information on the mid-range instruction set is available in the PIC16Cxxx Mid-Range MCU Family Reference Manual (DS3023).

Fig. A1.0 – Instruction Set of PIC16F84A

END OF PAPER