UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, SECOND SEMESTER MAY 2013

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	MICROELECTRONIC CIRCUITS
COURSE CODE:	EE523
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. A sheet containing some selected useful formulae is attached at the end.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(25 marks)***

Consider the IC amplifier shown in Figure-Q1.

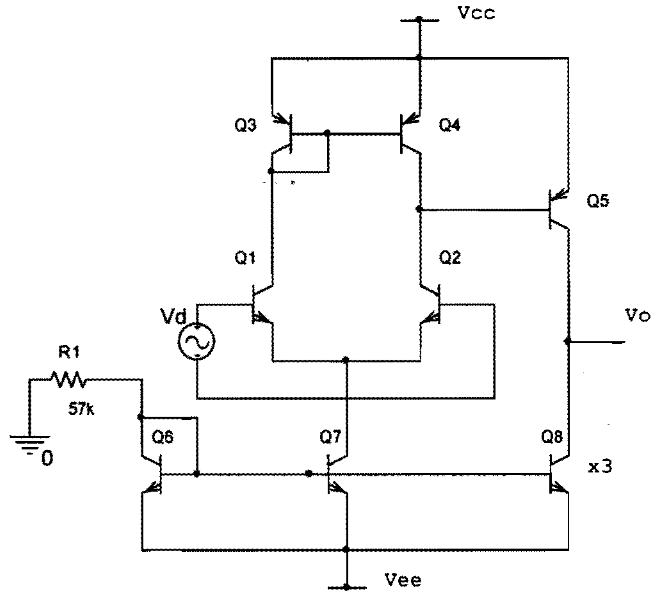

Figure-Q1

You may assume the following data.

$V_{A,PNP} = 70V$ $\beta_{PNP} = 75$ $V_{A,NPN} = 125V$ $\beta_{NPN} = 100$

$V_{CC} = 12V$ $V_{ee} = -12V$ $V_{BE} = 0.6V$

Calculate the following for this amplifier.

(a) Quiescent collector currents of the transistors.

(3 marks)

(b) Power dissipation of the amplifier at no signal.

(2 marks)

(c) Signal voltage gain $\frac{V_o}{V_d}$.

(10 marks)

(d) Input impedance and the output impedance.

(4 marks)

(e) Input common mode voltage range.

(6 marks)

QUESTION TWO *(25 marks)*

The block diagram of an uncompensated IC op-amp is shown in Figure-Q(2).

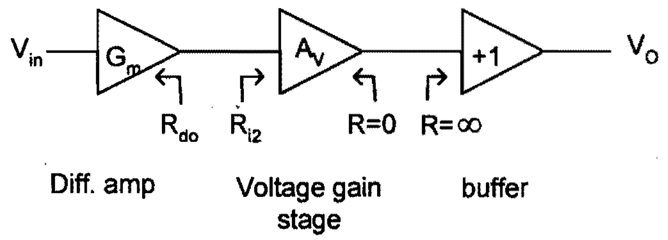

Figure-Q2

(a) Show to which points a capacitor is usually added to have dominant pole compensation.

(2 marks)

(b) If the compensation capacitor is 35pF, find the bandwidth of the op-amp after compensation.

$R_{do} = 1.5M$ $\quad$ $R_{i2} = 2M$ $\quad$ $A_V = -600$

Value of G_m is not given intentionally.

(7 marks)

(c) The DC gain of the op-amp is 100dB and is compensated as in (b).

(i) What is the bandwidth of the op-amp at unity gain?

(ii) The compensated op-amp is used with negative feedback to obtain a minimum bandwidth of 15 kHz. Find the limit of the maximum gain available and the feedback factor.

(8 marks)

(d) The current source in the differential amplifier stage supplies a current of $25\mu A$. If the maximum available output is $12V$, calculate the slew rate and the full power bandwidth of the compensated amplifier.

(8 marks)

QUESTION THREE *(25 marks)*

(a) Consider the emitter coupled differential pair shown in Figure-Q3.

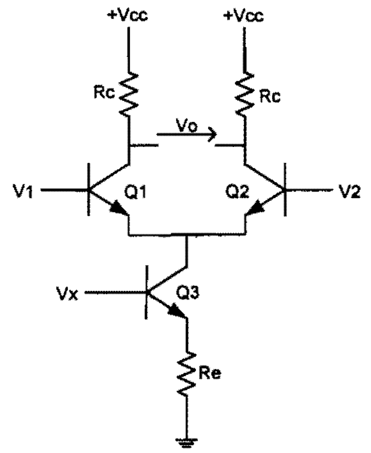

Figure-Q3

The input signal v_1 and v_2 are any voltage signals. Assuming that the transistors $Q1$ and $Q2$ are matched, show the circuit can be used as a multiplier giving $v_o = kv_x(v_1 - v_2)$, where k is a constant. In how many quadrant/s this multiplier is operational?

(10 marks)

(b) A multiplier can be assumed to have the input-output relationship $M = kXY$ where X and Y are the inputs and M is the output. The multiplier constant is k. Using this multiplier, show the implementation of the following with justification.

(i) A frequency doubler.

(ii) Square root function.

(ii) A divider.

(15 marks)

QUESTION FOUR (*25 marks*)

(a) The inverter shown in Figure-Q4 is fabricated in a $1.2\mu m$ CMOS technology.

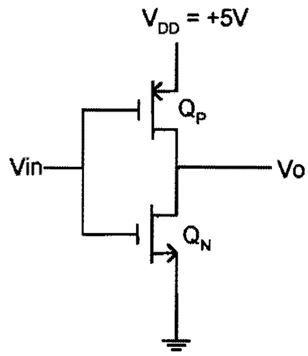

Figure - Q4

You may use the following process parameters and assume usual notation throughout.

$L_N = L_P = 1.2\mu m$ $W_N = 1.8\mu m$ $k_n' = 70\frac{\mu A}{V^2}$

$k_p' = 25\frac{\mu A}{V^2}$ $|V_{tp}| = V_{tn} = 0.8V$

(i) Show that the input threshold voltage V_{th} is given by

$$V_{th} = \frac{a(V_{DD}-|V_{tp}|)+V_{th}}{1+a} \quad \text{where} \quad a = \sqrt{\frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}}$$ (3 marks)

(ii) Calculate V_{th} and W_p if the devices are matched. (2 marks)

(iii) Find the values of V_{IH}, $V_{IL}$and the noise margins. (4 marks)

(iv) Assuming $W_p = 5.5\mu m$, calculate the output resistance of the inverter when $V_o = V_{OH}$. (3 marks)

(v) If the total effective load capacitance is $25fF$, estimate the propagation delay t_p assuming $W_p = 5.5\mu m$. (3 marks)

(vi) What is the power dissipation of the inverter if the load capacitance is $25fF$ and operated at a frequency of $100MHz$. (2 marks)

(b) Show the implementation of a 3-input NOR gate in CMOS technology. Provide transistor $\left(\frac{W}{L}\right)$ ratios in a $0.25\mu m$ process if $n = 2$ and $p = 5$.

(8 marks)

QUESTION FIVE (25 *marks*)

(a) A switched capacitor circuit is shown in Figure-Q5(a), which is driven by the two phase clock ϕ_1 and ϕ_2 with a cycle time of T_C.

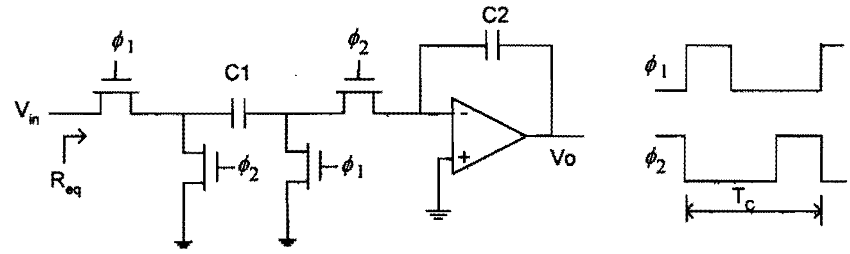

Figure - Q5(a)

(i) Derive expressions for $\frac{v_o}{v_{in}}$ and R_{eq}. (7 marks)

(ii) Show how you can get an inverted output v_o using the same circuit.

(3 marks)

(b) A circuit of an active low pass filter is shown in Figure-Q5(b).

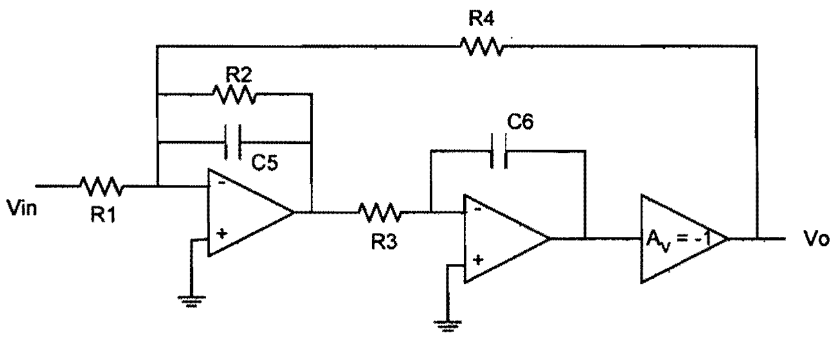

Figure-Q5(b)

The transfer function of the circuit is given by $-\frac{1}{R_3R_1C_5C_6\left(s^2+\frac{s}{C_5R_2}+\frac{1}{C_5C_6R_3R_4}\right)}$.

(i) Find the switched capacitor equivalent for this circuit using only two op-amps. Mark the clocks ϕ_1 and ϕ_2 clearly on the diagram.

(5 marks)

(ii) Calculate the capacitor values of your implementation to have a $3dB$ cutoff frequency of $10KHz$ when operating with a $100KHz$ clock. You may assume, $R_3 = R_4$ and,

$C_5 = C_6 = 10pF$ $\quad Q = \frac{1}{\sqrt{2}}$ $\quad K = 1$ $\quad \omega_{3dB} = \omega_0$

(10 marks)

SOME SELECTED USEFUL FORMULAE

MOSFET Equations:

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{in triode region}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \qquad \text{in saturation region}$$

Ebers-Moll Equation for i_C:

$$i_C = I_S\left(e^{v_{BE}/V_T} - 1\right) - \frac{I_S}{\alpha_R}\left(e^{v_{BC}/V_T} - 1\right)$$

Basic Inverter:

$$t_{PHL} = \frac{2C}{k_n'\left(\frac{W}{L}\right)_n (V_{DD}-V_{t,n})}\left[\frac{V_{t,n}}{(V_{DD}-V_{t,n})} + \frac{1}{2}ln\left(\frac{3V_{DD}-4V_{t,n}}{V_{DD}}\right)\right]$$

Low Pass Filter:

$$\text{Transfer Function} = \frac{K\omega_0^2}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2}$$