University of Swaziland
Faculty of Science and Engineering
Department of Electrical and Electronic Engineering

Main Examination 2013

Title of Paper: Analogue Design I

Course Number: EE321

Time Allowed: 3 hrs

Instructions:

1. Answer any four (4) questions.
2. Each question carries 25 marks.

This paper should not be opened until permission has been given by the invigilator.

This paper contains seven (7) pages including this page.

Question 1

a) Write some notes on the advantages of tuned amplifiers. [6]

b) For Fig. 1(b) below, use the following parameters: $R_B = 330k\Omega$, $R_L = 5k\Omega$, $R_{sig} = 5k\Omega$, $I_C = 1.3mA$, $V_T = 25mV$ and $\beta = 100$.

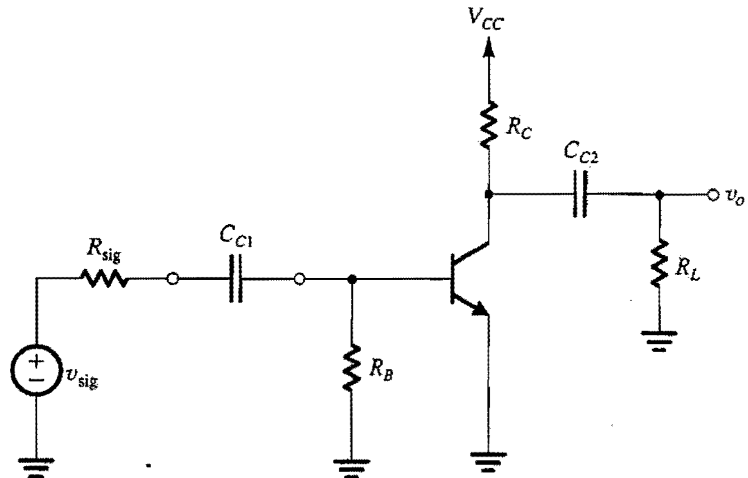

Fig. 1(b)

i) Draw the small signal model of the circuit. [2]

ii) Calculate the value of R_C so that the overall gain, $G_v = \frac{v_o}{v_{sig}} = -27V/V$. [8]

c) A particular small geometry BJT has $f_T = 5GHz$ and $C_\mu = 0.1pF$ when operated at $I_C = 0.5mA$ and $V_T = 25mV$.

i) Find g_m [1]

ii) When $\beta = 150$, find r_π and f_β. [2]

d) What is the frequency of oscillation of the astable multivibrator circuit shown in Fig. 1(d) below, where $V_{CC} = +5V$, $-V_{EE} = -5V$, $R_1 = 6.8k\Omega$, $R_2 = 6.8k\Omega$, $R = 10k\Omega$ and $C = 0.001\mu F$. [6]

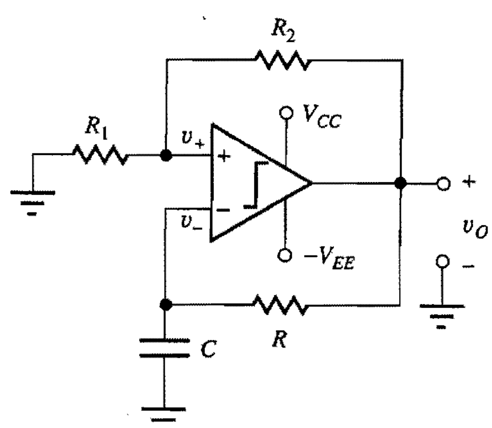

Fig. 1(d)

Question 2

a) Consider the emitter-follower amplifier of Fig. 2(a) for $I = 1mA$, $\beta = 100$, $V_T = 25mV$, $R_B = 100k\Omega$, $R_{sig} = 20k\Omega$ and $R_L = 1k\Omega$.

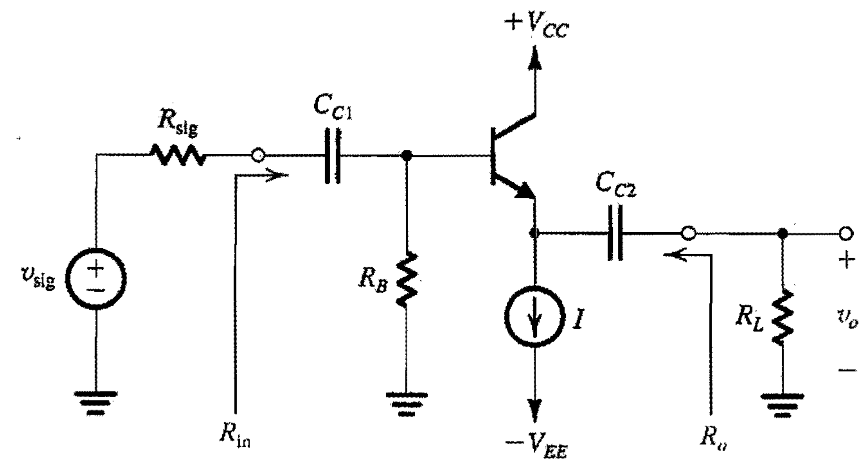

Fig. 2(a)

i) Find R_{in} [5]

ii) Find $\frac{v_o}{v_{sig}}$ [5]

b) Using an op-amp, design an inverting low-pass amplifier circuit which has an input resistance of $10k\Omega$, a low frequency voltage gain of -10, and a pole frequency of $10kHz$. Draw the appropriate diagram for your low-pass filter amplifier circuit. [10]

c) A compensating capacitor of $1000pF$ has a maximum charging current of $1mA$. What is the slew rate? [3]

d) What is the importance of amplifier compensation? [2]

Question 3

a) Consider the common-emitter amplifier shown in Fig. 3(a) under the following conditions: $R_{sig} = 5k\Omega$, $R_1 = 33k\Omega$, $R_2 = 22k\Omega$, $R_E = 3.9k\Omega$, $R_C = 4.7k\Omega$, $R_L = 5.6k\Omega$, $V_{CC} = 5V$, $r_o = 300k\Omega$, $\beta = 120$, dc collector current, $I_C = 0.3mA$, $V_T = 25mV$, $C_\mu = 1pF$, $f_T = 700MHz$ and $r_x = 50\Omega$. Find:

i) C_π [4]

ii) The upper $3-dB$ frequency, f_H. [10]

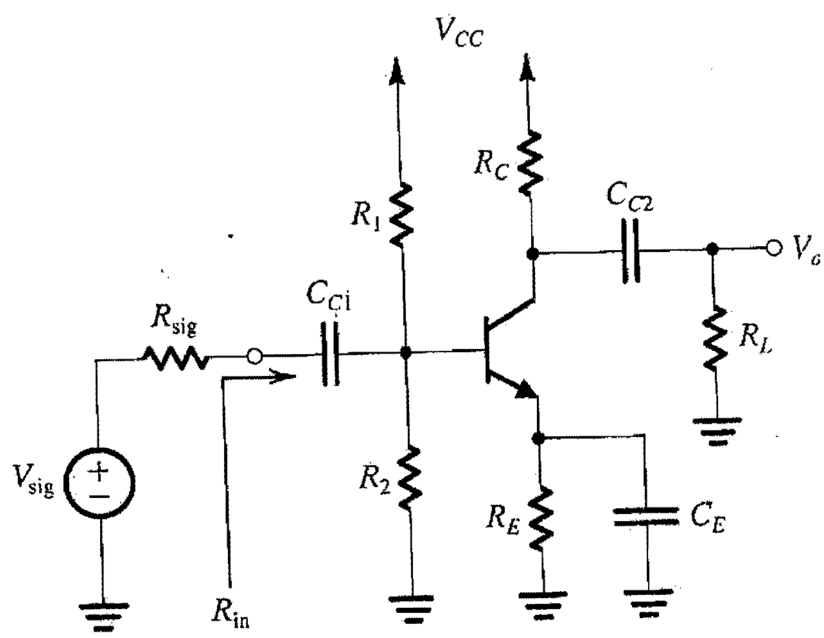

Fig. 3(a)

b) A coil having an inductance of $10\mu H$ is intended for applications around $1MHz$. Its Q_L is specified to be 200.

i) Find the equivalent parallel resistance, R_p. [2]

ii) What is the value of the capacitor required to produce resonance at $1MHz$? [3]

c) Suppose an amplifier has a differential mode gain of 2500 V/V and a CMRR of $80dB$. What is the output voltage if $v_1 = 5.001V$ and $v_2 = 4.999V$? [6]

Question 4

a) For the amplifier shown in Fig. 4(a), let $V_T = 25mV$, $\beta = 100$, $I_C = 0.245mA$, $R_{sig} = 1k\Omega$, $R_1 = 160k\Omega$, $R_2 = 300k\Omega$, $R_C = 22k\Omega$, $R_e = 3k\Omega$ and $R_L = 100k\Omega$. Find the values of:

i) R_{in} [5]

ii) $\frac{v_o}{v_{sig}}$ [5]

iii) What special name is given to resistor R_e? [1]

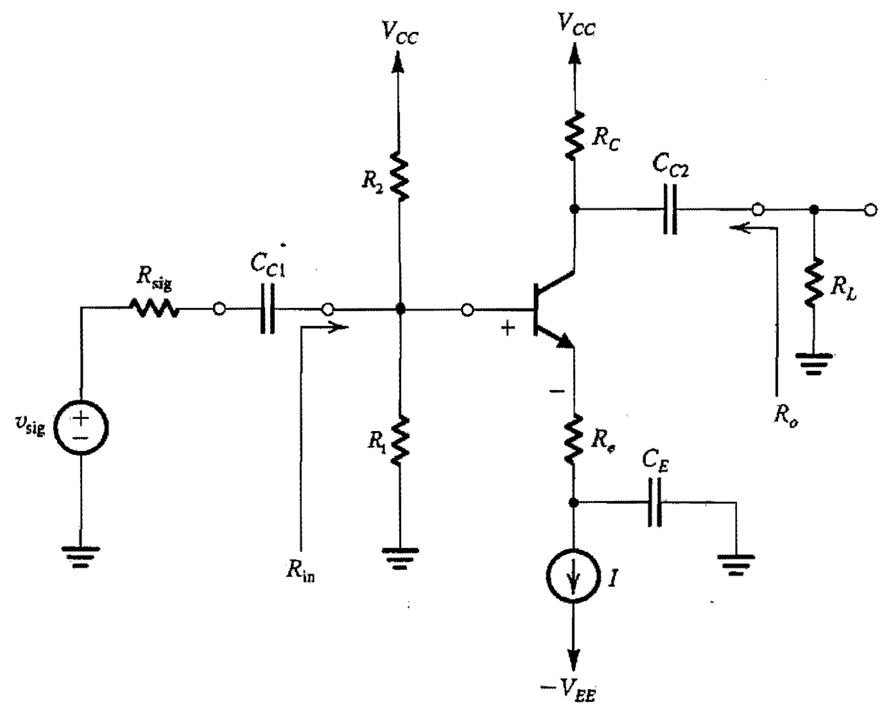

Fig. 4(a)

b) Write some short notes on Synchronous tuning; also include a basic circuit diagram showing the synchronously tuned amplifier and the frequency response of this amplifier. [10]

c) The op-amp in the bistable circuit shown in Fig. 4(c) has output saturation voltages of $\pm 13V$. Design the circuit to obtain threshold voltages of $\pm 5V$. For $R_1 = 10k\Omega$, find the value required for R_2. [4]

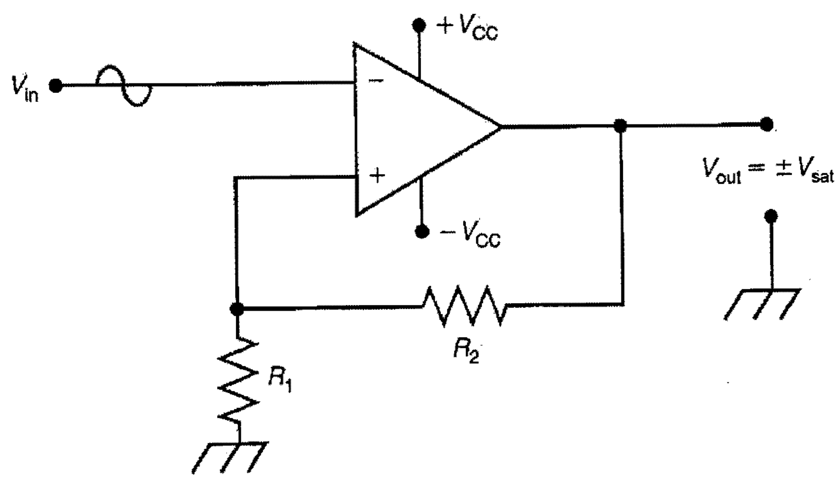

Fig. 4(c)

Question 5

a) Compare the properties of a common-emitter and a common-base amplifier. [6]

b) Derive an expression for the voltage gain for Fig. 5(b). Assume both transistors are well matched. [5]

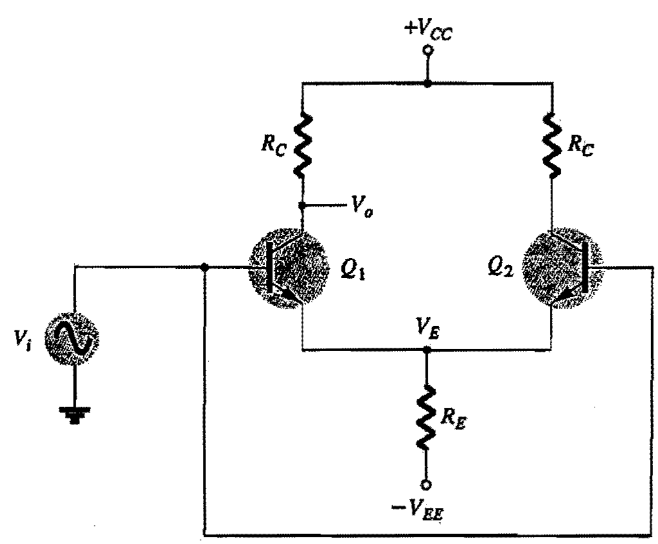

Fig. 5(b)

c) For the noninverting amplifier in Fig. 5(c) derive an expression its open loop gain, $A_v = \frac{V_{out}}{V_{in}}$. [6]

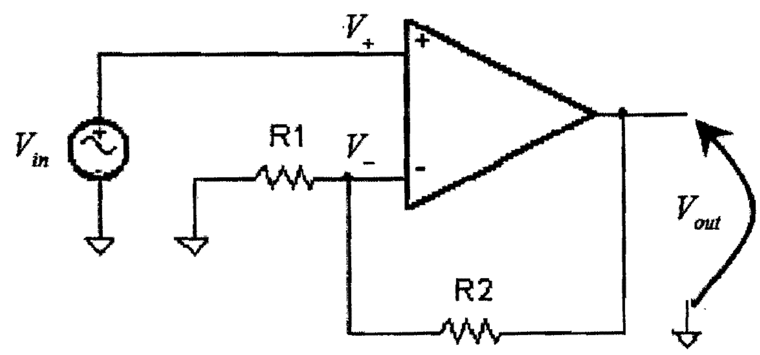

Fig. 5(c)

d) Design the voltage divider biased network of Fig. 5(d) to give $V_{CE} = 5V$ and $I_C = 750\mu A$. Take $\beta = 100$, $V_{BE} = 0.7V$, $V_{CC} = 15V$, $I_2 = 10I_B$, $I_1 = 9I_B$. Consider standard E12 range resistors for your final design. [8]

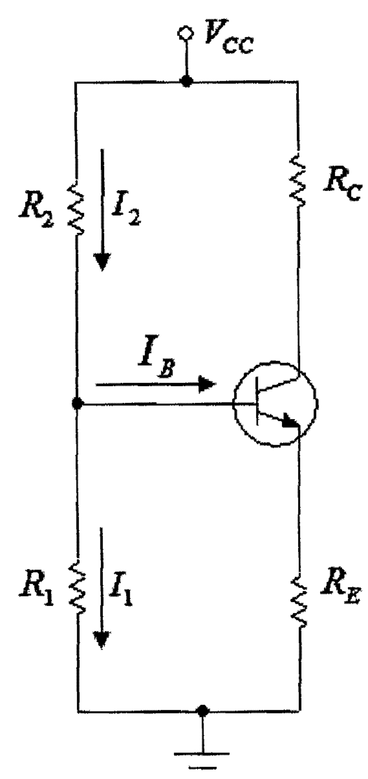

Fig. 5(d)