UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

November 2013
MAIN EXAMINATION

Title of the Paper: **Digital Systems I**
Course Number: **EE322**
Time Allowed: **Three Hours**.

Instructions:
1. To answer, pick Q1, Q2 & any others to sum a total of 100%
from questions in the following pages.
2. The answer is better neatly written in the space provided
in the question book.   Use the answer book as a scratch pad.
3. Must use the map and the table provided.
4. This paper has 7 pages, including this page.

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Compulsory for Q1 and Q2:

Q1. 10% What you see in Fig. Q1-1 is the view when 7404 inserted in a bread board; ie, the back side of the IC.   Answer the following questions:

1. Where is the pin #1, which pin #? for V_{cc}, which pin #? for Gnd.   Mark them on the figure Q1-1.
2. What is the V_{cc} voltage for this 74xx series? $V_{cc}=$

TTL

7404

7400

Fig. Q1-1

Q2. 10% Logic Circuit is working on indefinite H and L voltage.   For a TTL 74xx series, and for output, how high a voltage is H and how low is L?   What for input?   Give the following voltages:

1. $V_{OH}|_{min}=$ 2. $V_{OL}|_{max}=$
3. $V_{IH}|_{min}=$ 4. $V_{IL}|_{max}=$
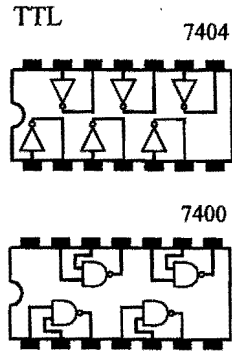
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Free to Choose for the Following Questions:

Q3. 10% Convert the following numbers from the given base to the bases indicated:

(a). decimal 115.22 to base 4 and hexadecimal

(b). hexadecimal 91.7 to decimal and binary

Q4. 10% Perform the subtraction with the following numbers using any complement. What is the total system number of digits? Check the answer by straight subtraction.

(a). $665-1700_{dec}$ (b). $11.01-110.1_{bin}$

Boolean Function Fundamentals:

Q5a 15% Transform the Boolean function below,

$$F(A,B,C) = \overline{B}(A+C)+C(\overline{A}+B),$$

into:

(i). Equation in SOP form, $F_s=\Sigma(---)_{hex}$, (ii). K-Map,
(iii). Equation in POS form, $F_p=\prod(---)_{hex}$, (iv). Truth table

$F_s=\Sigma($ $)_{hex}$

$F_p=\prod($ $)_{hex}$

AB-C	0	1
00		
01		
11		
10		

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Q5b 5% prove $F_p=\overline{F_s}$

Q6 10% Create a 4-bit reflected (Gray) code from the start byte, 1011.

B	1011		

Simplification:

Q7 10% With the help of a K-map, obtain the simplified expressions in (1) SOP, F_s and (2) POS, F_p of the following Boolean Function. Can you claim $F_s=F_p$ and explain why?

$$F(A,B,C) = A(BC + \bar{B}) + \overline{\overline{A}\overline{B}C}$$

AB-C	0	1
00		
01		
11		
10		

Q8 20% With the help of a K-map, obtain the simplified expressions in (1) SOP, F_s and (2) POS, F_p of the following Boolean Function, where d is the don't care case. Can you claim $F_s=F_p$ and explain why?

$$F(A,B,C,D) = A(BC + \bar{B}D) + \overline{AB}(\bar{C} + \bar{D})$$
$$d(A,B,C,D) = \bar{A}(B\bar{C} + CD) + A\bar{B}C\bar{D}$$

AB-CD	00	01	11	10
00				
01				
11				
10				

Combinational Logic Circuit:

Q9 20% Implement the Boolean function below with only NOR gates and nothing but NOR gates, yet complement inputs are available only at input terminals, nowhere else. The implementation must have its function support.

$$F(A,B,C,D) = (A + \overline{B})(\overline{A} + CD) + \overline{A}\,\overline{B}C$$

Q10 20% A switch system of 4 switches, A, B, C, and D is wired such as shown in Fig. Q8-1. A/B are always in compliment state and C/D as well; ie, A/B both in on or off state is prohibited, and C/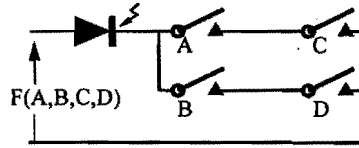D likewise. Design the switch system in logic circuit. If an LED is in series in the circuit, when will it turn on? Show all cases of the switch states to make LED light.

F(A,B,C,D)

Fig. Q8-1

AB	CD	F	AB	CD	F
00	00		10	00	
00	01		10	01	
00	10		10	10	
00	11		10	11	
01	00		11	00	
01	01		11	01	
01	10		11	10	
01	11		11	11	

Q11 20pts: Design a one digit adder of base 4 number. A carry is required. That is: the inputs of the circuit is two base 4 numbers, a total of 4 bits a, b, c, d, where the "ab" is augend and "cd" is addend, and the outputs are the sum S and the carry C. No circuit implementation is required but simplified functions.

A_2A_1	B_2B_1	F_2F_1	C_2C_1	A_2A_1	B_2B_1	F_2F_1	C_2C_1
00	00			10	00		
00	01			10	01		
00	10			10	10		
00	11			10	11		
01	00			11	00		
01	01			11	01		
01	10			11	10		
01	11			11	11		