UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2013

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

A circuit of a differential amplifier is shown in Figure-Q1.

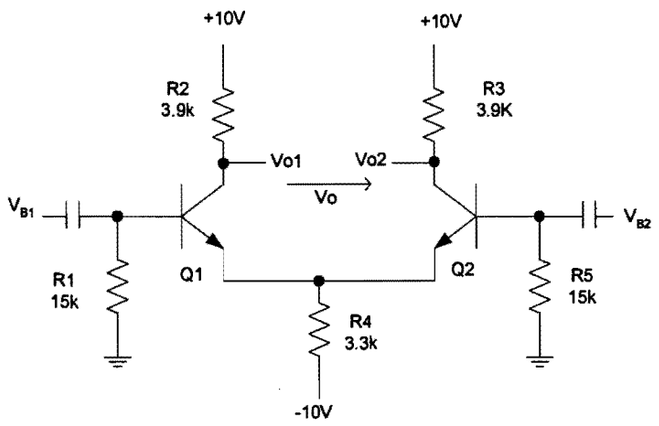

Figure - Q1

(a) Assuming that the transistors are of high gain type and matched, find the collector currents of the two transistors at no signal. Also find the voltages at the collectors and at the emitters.

(6 marks)

(b) When a differential input signal v_d is applied to the circuit, derive the expressions for the voltage gains $\frac{v_{o1}}{v_d}$, $\frac{v_{o2}}{v_d}$, $\frac{v_o}{v_d}$ and calculate their values.

(10 marks)

(c) Estimate the input offset voltage, input bias current and the input offset current of the amplifier using the following data.

Tolerance of resistors = $\pm 10\%$

Tolerance of scale currents = $\pm 20\%$

Tolerance of β = $\pm 20\%$

Value of β = 100

Assume that the tolerances of R_1, R_5 and R_4 have negligible effect.

(9 marks)

QUESTION TWO *(25 marks)*

Consider the NMOS amplifier shown in Figure-Q2. Assume that the devices Q_1 and Q_2 are matched.

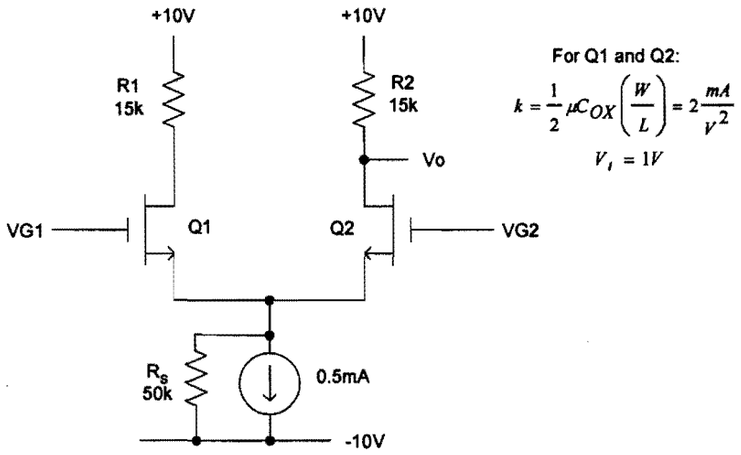

Figure - Q2

(a) If $V_{G1} = V_{G2} = 1V$, find the dc voltages at the drain and the source of the transistors.

(6 marks)

(b) If V_{G1} and V_{G2} are changed independently until $I_{D1} = 0.5mA$, calculate the value of differential input voltage applied.

(5 marks)

(c) When a common mode signal v_{cm} is applied to both inputs, find the common mode gain, $\frac{v_o}{v_{cm}}$ and $CMRR$. Prove any formula of the gain you use.

(8 marks)

(d) If the voltage drop across the current source V_S is such that $V_S \geq 2V$, find the maximum input common mode voltage range.

(6 marks)

QUESTION THREE ***(25 marks)***

(a) A current source implemented with BJTs is shown in Figure-Q3(a). The transistors are of high gain type and matched.

(i) Show that the current $I_{ref} = I_o e^{\frac{I_o R}{V_T}}$.

(4 marks)

(ii) Find the component values for this current source for an output current of $I_o = 100\mu A$. Assume that for the transistors used, $V_{BE} = 0.6V$ when the $I_C = 0.8mA$.

(5 marks)

(iii) Calculate the output resistance R_o if $V_A = 150V$ and the $\beta = 100$.

(4 marks)

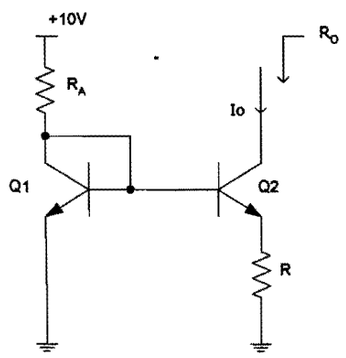

Figure-Q3 (a)

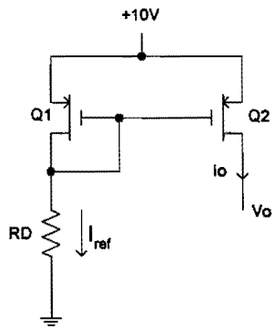

Figure-Q3 (b)

(b) A current mirror using PMOS devices is shown in Figure-Q3(b). Some of the parameters of the device and circuit are given below.

$L_1 = L_2 = 6\mu m$ $W_1 = 24\mu m$ $|V_t| = 2V$ $\mu C_{OX} = 40\frac{\mu A}{V^2}$

$V_A = 80V$ $I_o = 150\mu A$ $I_{ref} = 60\mu A$

(i) Calculate the value of W_2 proving any formula you use.

(4 marks)

(ii) Find the resistance of R_D.

(3 marks)

(iii) When $V_o = 4V$, find the actual value of the output current I_o.

(5 marks)

QUESTION FOUR (*25 marks*)

(a) Consider the CMOS amplifier shown in Figure-Q4(a), while assuming the following.

$K_1 = 4\frac{mA}{V^2}$ $K_2 = 2\frac{mA}{V^2}$ $K_3 = 2\frac{mA}{V^2}$ $I_{ref} = 0.85mA$
$|V_t| = 1V$ $|V_A| = 75V$

(i) Find the drain current of Q_3.

(4 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_i}$ and calculate its value.

(5 marks)

(iii) Give the limiting values of v_o which will ensure the operation of $Q_2$and Q_3 always to be in the saturation region.

(4 marks)

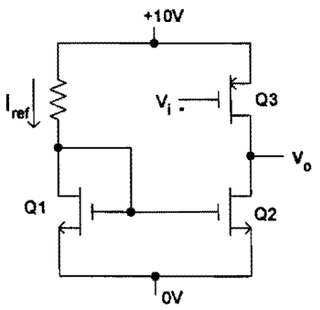

Figure - Q4(a)

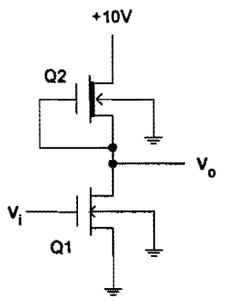

Figure - Q4(b)

(b) In the circuit shown in Figure-Q4(b), Q_1 and Q_2 are enhancement and depletion type devices respectively. You may assume the following data.

$W_1 = 100\mu m$ $L_1 = 5\mu m$ $W_2 = 5\mu m$ $L_2 = 20\mu m$ $V_{tE} = 2V$
$V_{tD} = -3V$ $\mu C_{OX} = 100\frac{\mu A}{V^2}$ $|V_A| = 75V$ $X = 0.1$

(i) Find the bias current at no signal.

(4 marks)

(ii) Draw the small signal equivalent circuit including the body effect and the output resistance. Hence derive the voltage gain $\left(\frac{v_o}{v_i}\right)$ and find its value.

(8 marks)

QUESTION FIVE (25 *marks*)

A block diagram of a synchronized frequency generator using a phased locked loop is shown in Figure-Q5. The phases of the signals are denoted by θ_i and θ_o.

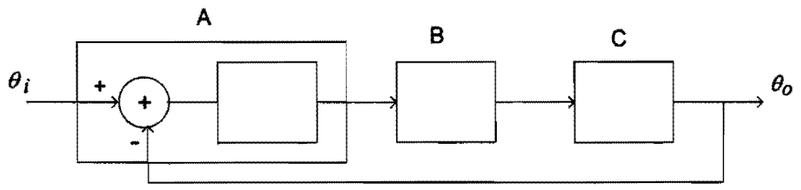

Figure - Q5

(i) Identify the function of each block A, B and C with marking the gains K_V $\frac{Hz}{V}$ and K_P $\frac{V}{rad}$ in the relevant blocks.

(5 marks)

(ii) If the system is designed with a loop filter having the transfer function $\frac{\tau_2 s+1}{\tau_1 s+1}$, draw the circuit of the filter and show how it is connected in the block diagram.

(8 marks)

(iii) Design the system using the following data with the filter mentioned in (ii).

$K_P = 3.82 \frac{V}{rad}$ $K_V = 1.67 \times 10^3 \frac{Hz}{V}$

Filter bandwidth = 500Hz

Damping factor = 0.707

A trial capacitance value which may be used is $0.1\mu F$. Also you may use,

$\tau_2 = \frac{2\sigma}{\omega_n} - \frac{1}{K}$ $\omega_n = \sqrt{\frac{K}{\tau_1}}$

(12 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.