Faculty of Science
Department of Electrical and Electronic Engineering
Main Examination 2015

Title of Paper : Analog Design II

University of Swaziland

Course Number : EE323

Time Allowed : 3 hrs

Instructions :

1. Read each of the SIX (6) questions carefully
2. Answer any FIVE (5) questions.
3. Each question carries 20 marks
4. Marks for each section are shown on the right hand margin

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The paper consists of eight (8) pages

Question 1 [20]

a) Define the following terms: [5]

i) Feedback
ii) Sensitivity
iii) Barkhausen Criterion
iv) Oscillator
v) Power Amplifier Efficiency

b) Give the effect of negative feedback on amplifier characteristics [8]

NB: Use *increase* and *decrease* to complete the table below

Characteristics	**type of feedback**			
	Current-series	**voltage-series**	**voltage-shunt**	**current-shunt**
Gain				
Bandwidth				
Input resistance				
Output resistance				

c) Design a ***Wien-bridge oscillator*** using op-amp to generate a sinusoidal waveform of frequency ***1 KHz.*** [7]

Question 2 [20]

a) The feedback amplifier shown in ***Figure 2.1*** makes use of an op – amp with an open – loop gain $\boldsymbol{A = 10^5}$.

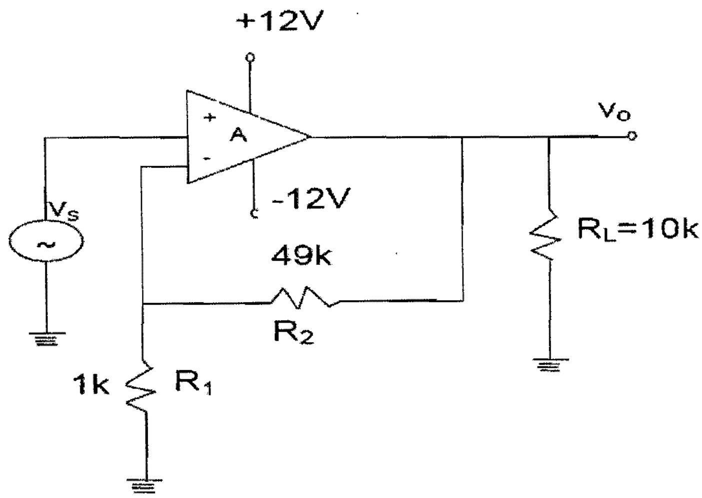

Figure 2.1

i) How much is the output voltage (v_o) for input signal $v_s = 2\,mV$ in the circuit shown [6]

b) ***Figure 2.2*** shows an op – amp circuit with voltage series through R_1 *and* R_2. The open – loop gain of the op – amp is $A = 10^4$ and input impedance is $100K\Omega$.

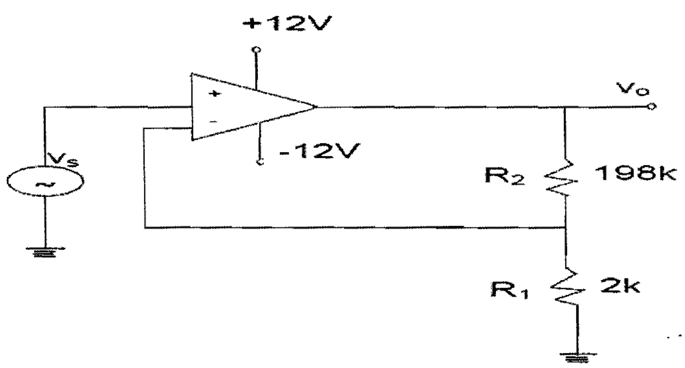

Figure 2.2

i) Find the gain and input impedance of the amplifier with feedback. [8]

c) An amplifier has a bandwidth of ***500 KHz*** and an open voltage gain of ***100.***

i) What should be the amount of negative feedback (β) if the bandwidth is extended to ***5 MHz***? [5]

ii) What will be the new gain after negative feedback is introduced? [1]

Question 3 [20]

For a series-series feedback BJT amplifier shown in ***Figure 3.1***. The input variable is the voltage v_1 and the output variable is the voltage v_2. Assume $\beta = 100, r_\pi = 2.5K\Omega, \alpha = \frac{\beta}{1+\beta}, r_e = \frac{\alpha}{g_m}$, $r_0 = \infty, r_x = 0, V_T = 25mV, R_1 = 100\Omega, R_2 = 1K\Omega, R_3 = 20K\Omega\ and\ R_4 = 10K\Omega$

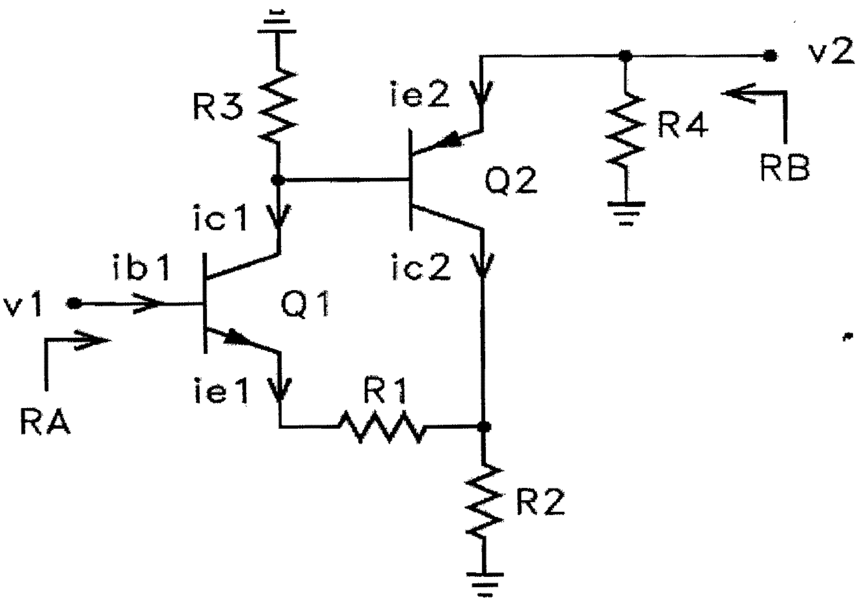

Figure 3.1

a. Redraw the circuit on ***Figure 3.1*** with the feedback path removed. NB: your diagram should be clearly labelled. [2]

b. Calculate the:

i. Transconductance $\frac{i_{e2}}{v_1}$ [6]

ii. Voltage gain v_2/v_1 [4]

iii. Input resistance R_A [4]

iv. Output resistance R_b [4]

Question 4 [20]

a) For the circuit of ***Figure 4.1.***

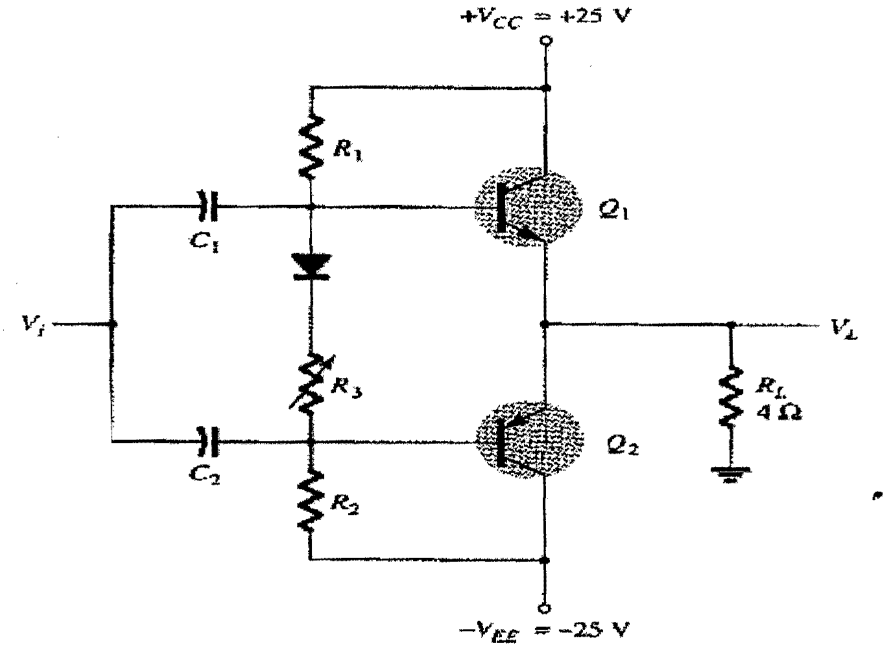

Figure 4.1

i) Calculate the:

- Output power [2]
- Input power [2]
- Power handled by each output transistor [2]
- Circuit efficiency for an input of 12 V_{rms} [1]

ii) Calculate the:

- Maximum input power [1]
- Maximum output power [1]
- Input voltage for maximum power operation [1]
- Power dissipated by the output transistors at this [1]

iii) Calculate the maximum power dissipated by the output transistors and the voltage at which this occurs [4]

b) For the Harmonic Distortion reading: $D_2 = 0.1, D_3 = 0.02, and\ D_4 = 0.01, with\ I_1 = 4\ A\ and\ R_c = 8\Omega$. Calculate the:

i) Total Harmonic Distortion [2]

ii) Fundamental power component [2]

iii) Total power [1]

Question 5 [20]

Figure 5.1 shows a series-shunt amplifier in which the three MOSFETs are sized to operate at $|V_{ov}| = 0.2\ V$. Let $|V_t| = 0.5V\ and\ |V_A| = 10\ V$. The current source utilizes single transistors and thus have output resistances equal to r_0.

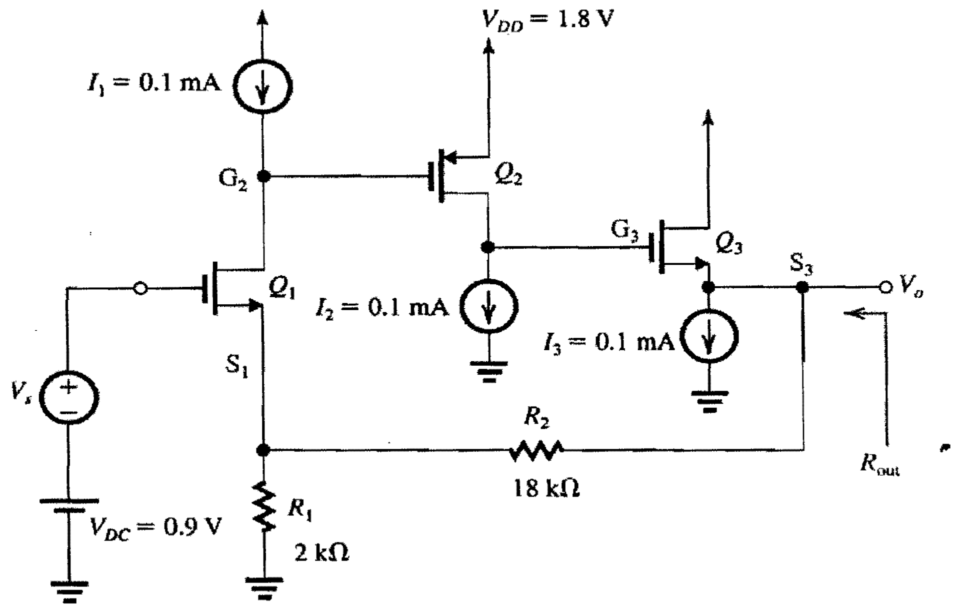

Figure 5.1

a) Assume the loop gain to be large, what do you expect the closed loop voltage $\frac{v_o}{v_s}$ to be approximately? [1]

b) If V_s has a zero dc component, find the dc voltages at nodes $S_1, G_{2,} S_{3,}\ and\ G_3$ [4]

c) Find the open – loop gain circuit. Calculate the gain of each of the three (3) stages and the overall voltage gain, A [15]

Question 6 [20]

a) Fill in the blank(s) with appropriate word(s) [10]

i) A MOSFET is a ____________ controlled ______________ carrier device.

ii) Enhancement type MOSFETs are normally ______________ devices while depletion type MOSFETs are normally ________________ devices.

iii) The Gate terminal of a MOSFET is isolated from the semiconductor by a thin layer of ____________ .

iv) The MOSFET cell embeds a parasitic ____________ in its structure.

v) The gate-source voltage at which the _____________ layer in a MOSFET is formed is called the _____________ voltage.

vi) The thickness of the _____________ layer remains constant as gate source voltage is increased beyond the ____________ voltage.

b) Determine the small-signal voltage gain, input and output resistances of a common-source amplifier. For the circuit shown in ***Figure 6.1***, the parameters are: $V_{DD} = 10V, R_1 = 70.9K\Omega, R_2 = 29{,}1K\Omega \; and \; R_D = 5K\Omega$. The transistor parameters are: $V_{TN} = 1.5V, K_n = 0.5mA/V^2, and \; \lambda = 0.01V^{-1}$. Assume $R_{si} = 4K\Omega$ and $g_m = 2k_n(V_{GSQ} - V_{TN})$

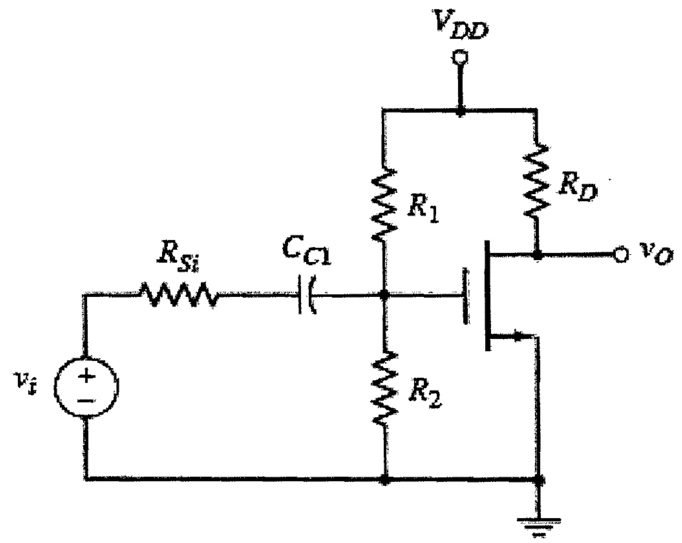

Figure 6.1