UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
Department of Electrical and Electronic Engineering

July 2015
SUPPLEMENTARY EXAMINATION

Title of the Paper:
Digital Systems II--EE324

Instructions:
1. The answer has to be written in the space provided in the question book. Consider only the material in the answer space be the answer. If need more space, the previous page is the best option. Use the answer book as a scratch pad. Both books must be marked with the student identity
2. There are 6 questions in the question book. Pick 5 and mark the not picked question with a big X in the answer space; or leave the grading person to pick according to the worst case first.
3. Time Allowed: Three Hours.
4. This paper has 7 pages, including this page.

DO NOT OPEN THE PAPER UNTIL
PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Registers, Counters, and memory:

Q1, 10pts: Given a 4-bit universal register, expand this into an 8-bit one and preserve all functions the 4-bit one has. Data lines and control lines must be explicitly marked.

Q2a, 10pts: Derive a state table from the given ASM chart on the right.

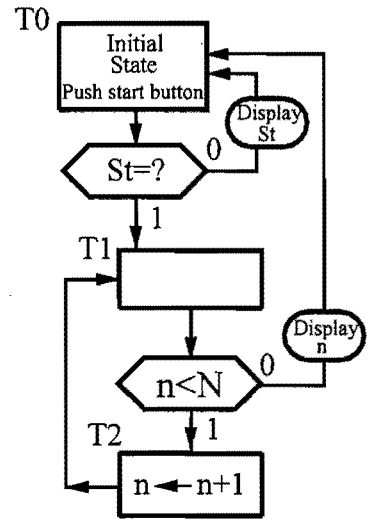**Q2b, 10pts:** Convert the given ASM chart on the right into a state diagram.

Fig. Q2-1

Analysis of a Given Sequential Circuit:

Q3, 20pts: A given sequential circuit is shown in Fig. Q3-1. Analyze the circuit and give the circuit (i) (8 pts), state diagram, (ii) (8pts), state table, and (iii) (4 pts), Is the circuit self-starting and/or self-correcting. Give the reason for the answer.
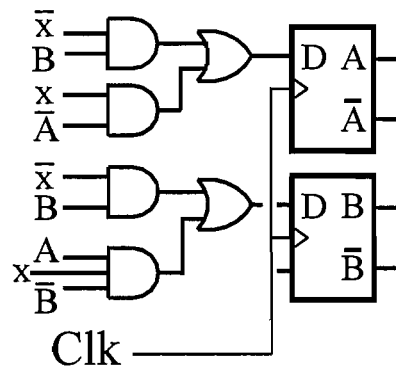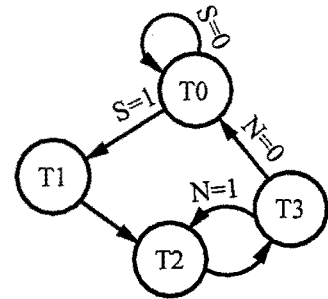

Fig. Q3-1

Control Circuit Design

Q4, 20pts: Shown below is a 4-state state diagram of a control unit where control inputs are S and N. Design the control circuit by the sequence register and decoder structure with two D-ffs G_2 and G_1 for the sequence register. Use the decoder output as conditions for the present states.

Fig, Q4-1

Register-Transfer Circuit:

Q5, 20 pts: It is required to exchange data between two blocks of data in a RAM: one data block, DB1(001A, 002A), the other data block, DB2 (003E, 004E). Use any other space of this RAM(0000, FFFF) as the intermediate storage device; this intermediate storage address must be specified. (Note: All the pair of numbers in the bracket are the address in Hex number from the start point to the end.)

(a) 10pts: Draw the hardware circuit for this system. Of course, MAR, MBR, and memory unit must be included.

(b) 10pts: Use registry language to describe the operation. (hint: it is better to design an ASM chart first, Q6)

Practical Design
  Q6, 20pts: Design the ASM chart of Q5.