

UNIVERSITY OF SWAZILAND
MAIN EXAMINATION, FIRST SEMESTER
DECEMBER 2014

FACULTY OF SCIENCE AND ENGINEERING

**DEPARTMENT OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

TITLE OF PAPER: ANALOGUE DESIGN III
COURSE CODE: EE421

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any **FOUR** questions.
Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

**THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION
HAS BEEN GIVEN BY THE INVIGILATOR**

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE (25 marks)

A BJT differential amplifier is shown in Figure-Q1.

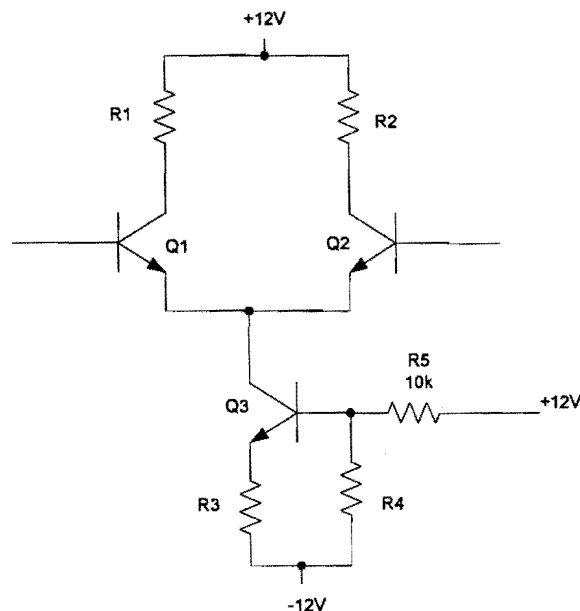


Figure-Q1

- (a) When there is no input signal, the collector currents in each of the transistors Q_1 and Q_2 are 1.2mA . Assuming that the transistors are of high gain type and matched, calculate the values of R_1 , R_2 , R_3 and R_4 . Hence select practical values for these resistors from the E12 range. You may use,

$$\text{Collector voltage of } Q_1 \text{ and } Q_2 \approx 5.5\text{V}$$

$$\text{Emitter voltage of } Q_3 \approx -10\text{V}$$

(8 marks)

- (b) (i) If two dc voltages V_{B1} and V_{B2} are applied to the base of Q_1 and Q_2 respectively, show that the emitter current of Q_1 is given by, $\frac{2.4}{1+e^{40V_D}} \text{ mA}$ where $V_D = (V_{B2} - V_{B1})$ volts. You may assume that $\alpha = 1$.
- (ii) Evaluate the collector current and the collector voltage of Q_1 and Q_2 , if $V_{B1} = 100\text{mV}$ and $V_{B2} = 80\text{mV}$.

(12 marks)

- (c) If $V_{CE(\text{sat})} = 0.2\text{V}$ for the three transistors, find the maximum and minimum common mode input voltages.

(5 marks)

QUESTION TWO (25 marks)

An enhancement mode NMOS amplifier shown in Figure-Q2. Assume that the devices Q_1 and Q_2 are matched.

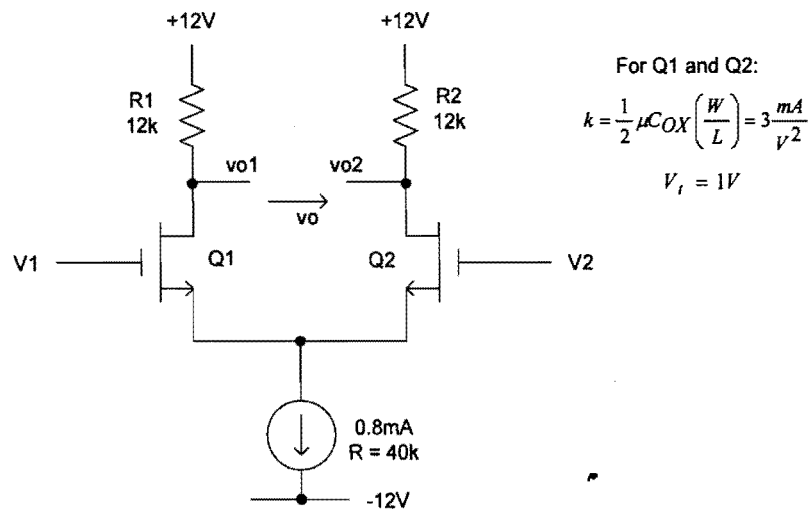


Figure - Q2

- (a) When no ac signal is present, calculate the differential input voltage applied if the drain voltage of Q_2 is 12V. (6 marks)
- (b) Draw the differential half circuits for the ac signals and derive expressions for the voltage gains $\frac{v_{o1}}{v_d}$, $\frac{v_{o2}}{v_d}$, $\frac{v_o}{v_d}$ and calculate their values. The differential input signal voltage is denoted by v_d and assume that the bias voltages $V_1 = V_2 = 0$. (9 marks)
- (c) If a common mode input signal v_{cm} is applied, derive an expression for the common mode gain $\frac{v_{o1}}{v_{cm}}$ using the half circuits and find its value. What is the $CMRR$ of this circuit? (7 marks)
- (d) When fabricating this circuit, a mismatch is found in R_1 , R_2 , Q_1 and Q_2 . Estimate the resulting input offset voltage using the following data.

$$\text{Tolerance in resistors} = \pm 2\%$$

$$\text{Tolerance in } \left(\frac{W}{L}\right) \text{ ratio} = \pm 5\%$$

(3 marks)

QUESTION THREE (25 marks)

- (a) A circuit of a BJT current source with matched transistors is shown in Figure-Q3(a). You may assume that the $\beta = 40$ and $V_A = 75V$.
- (i) In a diagram, mark the currents in all transistors in terms of I_O and β . Hence derive an expression for the current I_O . (6 marks)
- (ii) Calculate the values of R_1 and R_2 if the output current $I_O = 1.2mA$. (4 marks)
- (iii) What is the output resistance R_o ? If the output voltage $V_o = 5V$, find the actual value of the output current I_O . (7 marks)

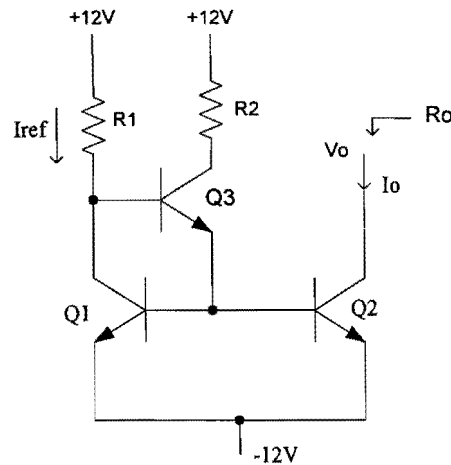


Figure-Q3(a)

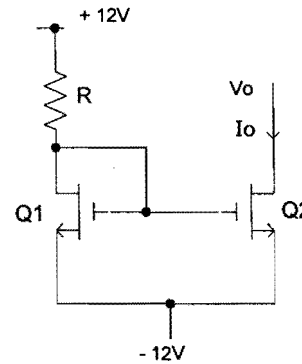


Figure-Q3(b)

- (b) A current mirror implemented with NMOS devices is shown in Figure-Q3(b). Some useful data regarding this circuit is given below.

$$L_1 = L_2 = 5\mu m \quad W_2 = 50\mu m \quad |V_t| = 2V \quad \mu C_{OX} = 60 \frac{\mu A}{V^2}$$

$$V_A = 75V \quad I_o = 200\mu A \quad I_{ref} = 40\mu A$$

- (i) Calculate the value of W_1 proving any formula you use. (5 marks)
- (ii) Find the value of the resistance R . (3 marks)

QUESTION FOUR (25 marks)

- (a) An integrated circuit amplifier is shown in Figure-Q4(a). Assume that the transistors are of high gain and matched. You may assume that the $\beta = 100$ and $V_A = 75V$.
- Identify the function of Q_1 and Q_3 . Calculate the collector current of Q_1 at no signal. (3 marks)
 - Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value. (5 marks)
 - If this amplifier drives a load of $100k$, what is the resulting voltage gain? (3 marks)
 - Derive the input impedance R_{in} and the output impedance R_o . (3 marks)

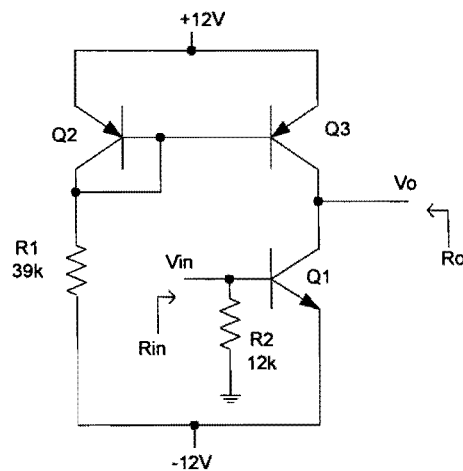


Figure-Q4(a)

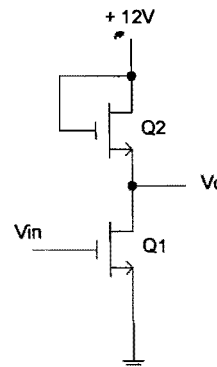


Figure-Q4(b)

- (b) An amplifier implemented with enhancement type NMOS transistors is shown in Figure-Q4(b). Some useful device parameters are given below.
- $$W_1 = 150\mu m \quad L_1 = 20\mu m \quad W_2 = 15\mu m \quad L_2 = 80\mu m \quad V_t = 2V$$
- $$\mu C_{OX} = 200 \frac{\mu A}{V^2}$$
- Calculate the drain current of Q_1 , if $V_o = 6V$ at no signal. Also find the dc input voltage required in this case. Prove any formula you use. (4 marks)
 - Draw the small signal equivalent circuit for the amplifier. Hence derive an expression for the voltage gain $\left(\frac{v_o}{v_{in}}\right)$ and calculate its value. (7 marks)

QUESTION FIVE (25 marks)

A voltage regulator circuit is shown in Figure-Q5.

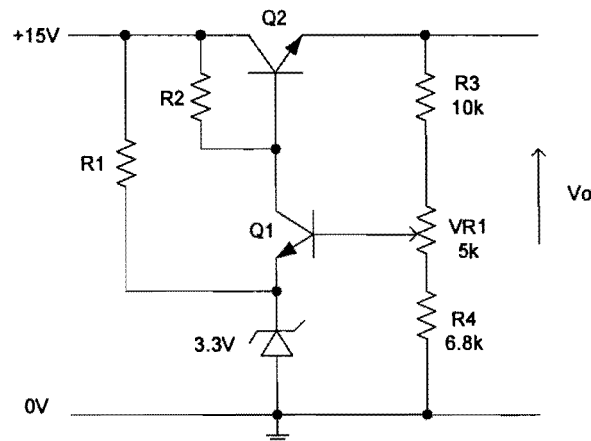


Figure-Q5

- (i) Calculate the output voltage range of this regulator. (6 marks)
- (ii) Show a circuit of an active current limit for this circuit. Also find the values of the resistor(s) with power ratings in your circuit assuming a maximum load current of 1.5A. (5 marks)
- (iii) Calculate the maximum power dissipation in Q_2 for a maximum load current of 1.5A. (4 marks)
- (iv) Find the values of R_1 and R_2 for the following data,
 - maximum load current = 1.5A
 - minimum collector current of $Q_1 = 10mA$
 - minimum current of zener diode = 5mA
 - $\beta_{Q2} = 15$(5 marks)
- (v) Find the maximum power dissipation in R_1 , R_2 and the zener diode. (5 marks)

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = \mu_n C_{ox} \frac{W}{L} \left[(v_{GS} - v_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \text{ in triode region}$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - v_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - v_t)^2 (1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

$$V_A = \frac{1}{\lambda}$$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.