UNIVERSITY OF SWAZILAND

SUPPLIMENTERY EXAMINATION

JULY 2015

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

A differential amplifier circuit implemented with BJTs, is shown in Figure-Q1.

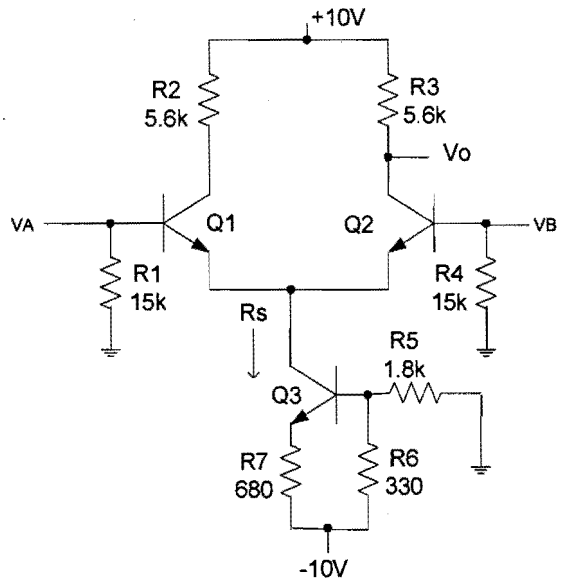

Figure-Q1

(a) If the transistors are of high gain type, calculate the collector currents and collector voltages of each transistor at no signal.

(6 marks)

(b) Assuming a signal source v_d is differentially connected to the inputs (ie, $v_d = v_A - v_B$), draw the differential half circuit for ac signals and find the voltage gain $\frac{v_o}{v_d}$ deriving any formula you use.

(7 marks)

(c) Draw the common mode half circuit for ac signals and calculate the common mode gain at the output v_o. What is the CMRR in dB? Derive any formula you use. Assume the resistance $R_S = 600k$

(8 marks)

(d) Calculate the differential input resistance of the amplifier. You may use, $\beta_{Q1} = \beta_{Q2} = 100$.

(4 marks)

QUESTION TWO *(25 marks)*

(a) Consider the Widlar current source shown in Figure-Q2(a). The transistors $Q_1$and $Q_2$are matched and of high gain type.

(i) Derive a relationship between I_o and I_{ref}.

(6 marks)

(ii) Find the value of R_F if the output current of the source is $130\mu A$, using the following data.

$V_{CC} = 10V$ $V_{BE1} = 0.6V$ $R = 560\Omega$

(6 marks)

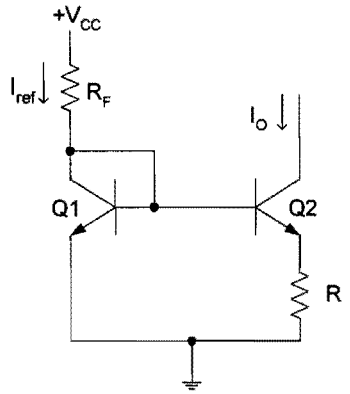

Figure-Q2(a)

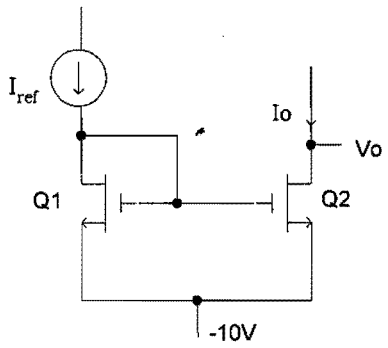

Figure-Q2(b)

(b) A current mirror designed with NMOS devices is shown in Figure-Q2(b). You may assume the following device parameters.

$L_1 = L_2 = 5\mu m$ $W_1 = 15\mu m$ $W_2 = 50\mu m$ $V_t = 2V$

$\mu C_{ox} = 60\frac{\mu A}{V^2}$ $I_{ref} = 40\mu A$

(i) Find the value of V_{GS}.

(4 marks)

(ii) Calculate the value of the output current I_o.

(5 marks)

(iii) What is the minimum value of the output voltage V_o?

(4 marks)

QUESTION THREE ***(25 marks)***

(a) An IC amplifier is shown in Figure-Q3(a). Assume that the transistors are of high gain type with Q_1 and Q_2 are matched.

(i) Find the value of R if the collector current of Q_3 is $350\mu A$.

(5 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value.

$V_A = 80V$ $\beta = 100$

(5 marks)

(iii) Find the input impedance of the amplifier.

(2 marks)

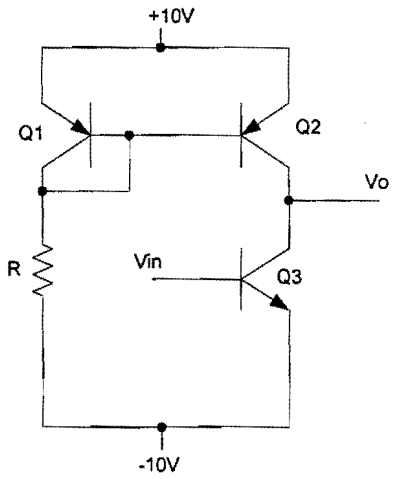

Figure-Q3(a)

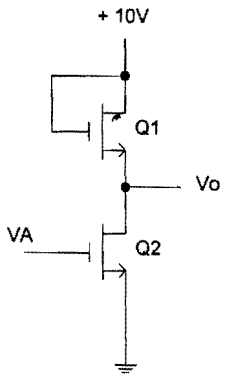

Figure-Q3(b)

(b) An amplifier implemented with enhancement type NMOS devices is shown in Figure-Q3(b). Assume the following process parameters for the devices.

$L_2 = 10\mu m$ $L_1 = 40\mu m$ $W_2 = 150\mu m$ $W_1 = 10\mu m$

$V_t = 3V$ $\mu C_{OX} = 100\frac{\mu A}{V^2}$

(i) If V_A is given a dc voltage of $3.5V$, find the dc voltage at the output V_o and the current flowing in Q_1.

(6 marks)

(ii) An ac signal of 100mVp-p superimposed on a 3.5V dc level is applied to the input. Draw the small signal equivalent circuit and calculate the output ac signal voltage.

(7 marks)

QUESTION FOUR (*25 marks*)

Consider the cascode amplifier shown in Figure-Q4.

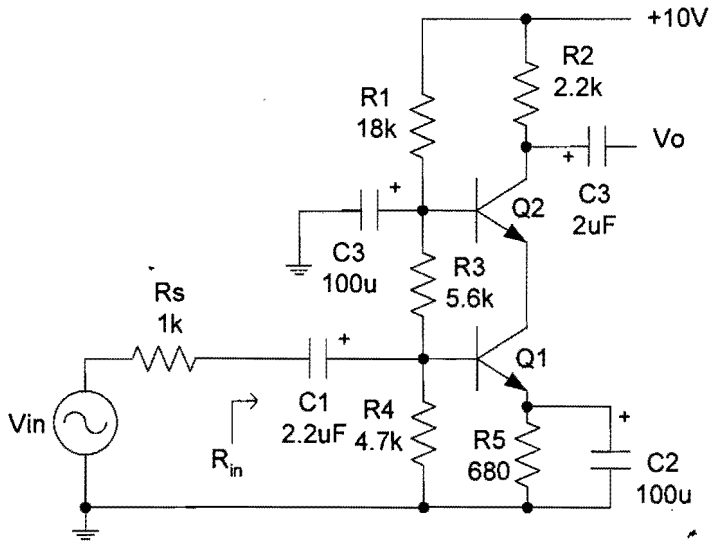

Figure-Q4

(i) If the transistors are identical and of high gain type, find the collector currents and the collector voltages of each transistor under no signal.

(8 marks)

(ii) Derive an expression for the mid-band gain $\frac{v_o}{v_{in}}$, and find its value. Assume that the $\beta = 100$ and may neglect the Early effect.

(12 marks)

(iii) Find an expression for the input impedance R_{in} and calculate its value for ac signals.

(5 marks)

QUESTION FIVE (25 *marks*)

A dc voltage regulator circuit is shown in Figure-Q5.

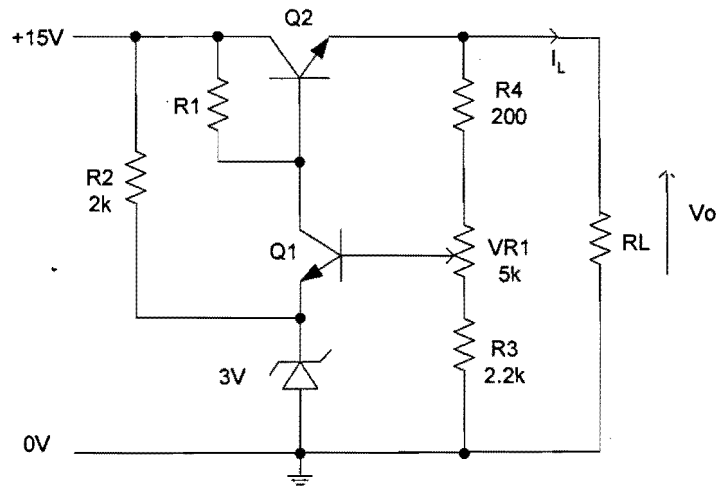

Figure-Q5

(i) What are the maximum and minimum values of V_o?

(5 marks)

(ii) Find the maximum value of load current if the maximum power dissipation in Q_2 is $20W$.

(5 marks)

(iii) Suggest an over current protection circuit for the regulator output, based on an active device and also determine the necessary component values with power rating.

(5 marks)

(iv) Estimate the value of R_1 and its power rating if $\beta_{Q2} = 20$ and $I_{C1} \geq 15mA$.

(5 marks)

(v) Find the maximum power dissipation in the zener diode.

(5 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L} \left[(v_{GS} - v_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$ in triode region

$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - v_t)^2 (1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.