

Faculty of Science
Department of Electrical and Electronic Engineering
Main Examination 2015

Title of Paper : **Digital Systems I**

Course Number : **EE322**
University of Swaziland

Time Allowed : **3 hrs**

Instructions :

- 1. Answer all four (4) questions**
- 2. Each question carries 25 marks**

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BEEN GIVEN BY THE INVIGILATOR**

The paper consists of five (6) pages including the cover page

Question 1 [25]

a) Convert the following decimal numbers to the base indicated

i. 7562 to octal [2]

ii. 1938 to hexadecimal [2]

iii. 175 to binary [1]

b) Show the following operations using 2's complement:

i. $1011001 - 1000011$ [2]

ii. $0.1001 - 0.0101$ [3]

c) Using postulates and theorems of Boolean algebra, reduce the combinational circuit in figure 1.1 to a minimum number of literals. Draw the circuit using one gate. [15]

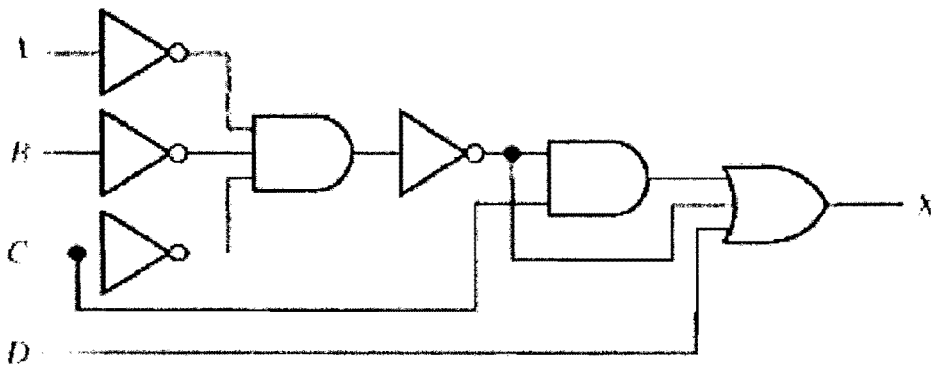


figure 1.1

Question 2 [25]

a) What do you understand about the following terms as used in digital design:

- i) Encoder [1]
- ii) Decoder [1]
- iii) Multiplexer [1]
- iv) Demultiplexer [1]
- v) Combinational circuit [2]
- vi) Sequential circuit [2]
- vii) Magnitude comparator [2]

b) A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (*a, b, c, d, e, f, g*) select the corresponding segments in the display, as shown in Figure 2.1. The numeric display chosen to represent the decimal digit is shown Figure 2.2. Design this decoder using a minimum number of gates. The six invalid combinations should result in a blank display. [15]

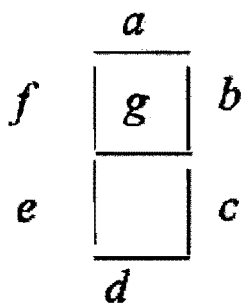


figure 2.1

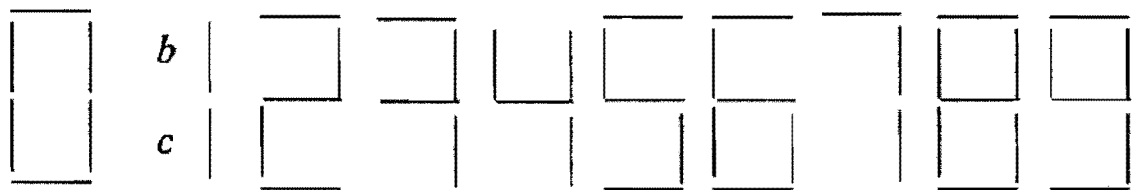


figure 2.2

Question 3 [25]

a) Implement the following Boolean function with a multiplexer:

$$F(A, B, C, D) = (0, 1, 3, 4, 8, 9, 15)$$

[10]

b) From the following state diagram, figure 3.1 create the state table, and corresponding circuit using D flip-flops. [15]

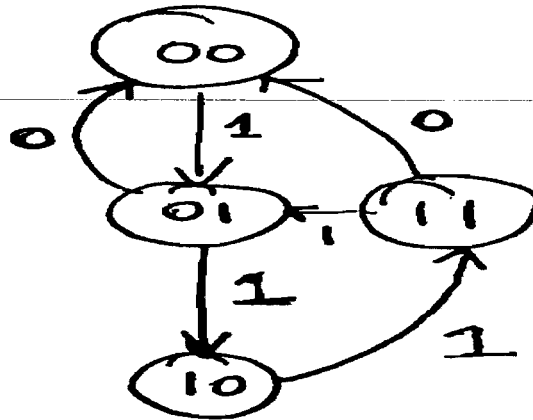
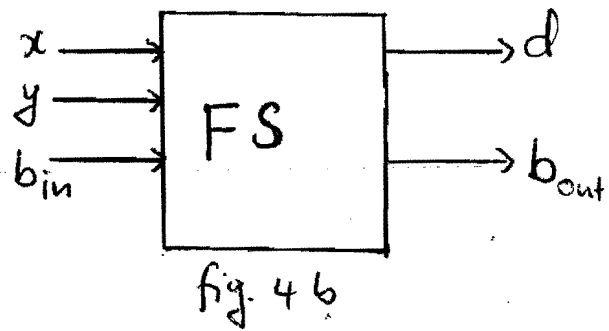
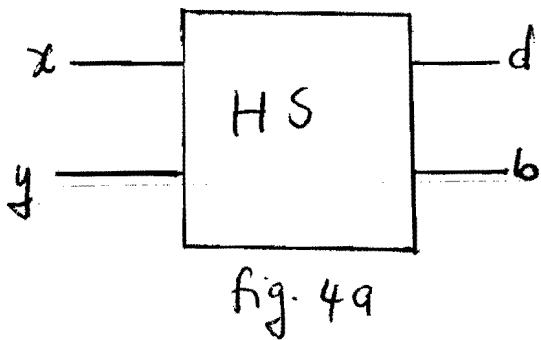


figure 3.1

Question 4 [25]

a) The graphical symbols of a half-subtractor (HS) and a full-subtractor (FS) for computing $b, d = x - y$, where b stands for borrow and d stands for difference are shown below:



- i) Derive the truth table and minimal cost Sum of Product (SOP) implementation for the HS. [4]
- ii) Derive the truth table and a minimal cost SOP implementation for the FS [7]
- iii) Show how to build a FS from two HS blocks and an additional gate. [5]

- b) Draw a circuit using *AND*, *OR*, and *NOT* gates to implement the function F specified by the truth table shown below. Try to minimize the number gates used.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0