# University of Swaziland <br> Faculty of Science <br> Department of Electrical and Electronic Engineering Supplementary Examination 2016 

| Title of Paper | $:$ | Analogue Design II |
| :--- | :--- | :--- |
| Course Number | $:$ | EE323 |


| Time Allowed | $: \quad 3 \mathrm{hrs}$ |
| :--- | :--- |
| Instructions | $:$ |

1. This paper contains five (5) questions
2. Answer all questions
3. Each question carries $\mathbf{2 0}$ marks

# THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR 

The paper consists of six (6) pages

## Question 1 [20]

a) Define the following terms:
i) Feedback
ii) Sensitivity
iii) Barkhausen Criterion
iv) Oscillator
v) Power Amplifier Efficiency
b) Give the effect of negative feedback on amplifier characteristics

NB: Use increase and decrease to complete the table below

| Characteristics | type of feedback |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
|  | Current-series | voltage-series | voltage-shunt current-shunt |  |
| Gain |  |  |  |  |
| Bandwidth |  |  |  |  |
| Input resistance |  |  |  |  |
| Output resistance |  |  |  |  |

c) Design a Wien-bridge oscillator using op-amp to generate a sinusoidal waveform of frequency $1 \mathbf{K H z}$.

## Question 2 [20]

For a series-series feedback BJT amplifier shown in Figure 2.1. The input variable is the voltage $v_{1}$ and the output variable is the voltage $v_{2}$. Assume $\beta=100, r_{\pi}=2.5 \mathrm{~K} \Omega, \alpha=\frac{\beta}{1+\beta}, r_{e}=\frac{\alpha}{g_{m}}$, $r_{0}=\infty, r_{x}=0, V_{T}=25 \mathrm{mV}, R_{1}=100 \Omega, R_{2}=1 \mathrm{~K} \Omega, R_{3}=20 \mathrm{~K} \Omega$ and $R_{4}=10 \mathrm{~K} \Omega$


Figure 2.1
a. Redraw the circuit on Figure 2.1 with the feedback path removed.

NB: your diagram should be clearly labelled.
b. Calculate the:
i. Transconductance $\frac{i_{e_{2}}}{v_{1}}$
ii. Voltage gain $v_{2} / v_{1}$
iii. Input resistance $R_{A}$
iv. Output resistance $R_{b}$

## Question 3 [20]

a) For the circuit of Figure 3.1.


Figure 3.1
i) Calculate the:

- Output power
- Input power
- Power handled by each output transistor
- Circuit efficiency for an input of $12 V_{r m s}$
ii) Calculate the:
- Maximum input power
- Maximum output power
- Input voltage for maximum power operation
- Power dissipated by the output transistors at this
iii) Calculate the maximum power dissipated by the output transistors and the voltage at which this occurs
b) For the Harmonic Distortion reading: $D_{2}=0.1, D_{3}=0.02$, and $D_{4}=0.01$, with $I_{1}=$ $4 A$ and $R_{c}=8 \Omega$. Calculate the:
i) Total Harmonic Distortion
ii) Fundamental power component
iii) Total power


## Question 4 [20]

Figure 4.1 shows a series-shunt amplifier in which the three MOSFETs are sized to operate at $\left|V_{o v}\right|=0.2 \mathrm{~V}$. Let $\left|V_{t}\right|=0.5 \mathrm{~V}$ and $\left|V_{A}\right|=10 \mathrm{~V}$. The current source utilizes single transistors and thus have output resistances equal to $r_{0}$.


Figure 4.1
a) Assume the loop gain to be large, what do you expect the closed loop voltage $\frac{v_{o}}{v_{s}}$ to be approximately?
b) If $V_{5}$ has a zero dc component, find the dc voltages at nodes $S_{1}, G_{2}, S_{3}$, and $G_{3}$
c) Find the open - loop gain circuit. Calculate the gain of each of the three (3) stages and the overall voltage gain, A

## Question 5 [20]

a) Fill in the blank(s) with appropriate word(s)
[10]
i) A MOSFET is a $\qquad$ controlled $\qquad$ carrier device.
ii) Enhancement type MOSFETs are normally $\qquad$ devices while depletion type MOSFETs are normally $\qquad$ devices.
iii) The Gate terminal of a MOSFET is isolated from the semiconductor by a thin layer of $\qquad$ _.
iv) The MOSFET cell embeds a parasitic $\qquad$ in its structure.
v) The gate-source voltage at which the $\qquad$ layer in a MOSFET is formed is called the $\qquad$ voltage.
vi) The thickness of the $\qquad$ layer remains constant as gate source voltage is increased beyond the $\qquad$ voltage.
b) Determine the small-signal voltage gain, input and output resistances of a commonsource amplifier. For the circuit shown in Figure 5.1, the parameters are: $V_{D D}=$ $10 \mathrm{~V}, R_{1}=70.9 \mathrm{~K} \Omega, R_{2}=29,1 K \Omega$ and $R_{D}=5 K \Omega$. The transistor parameters are: $V_{T N}=1.5 \mathrm{~V}, K_{n}=0.5 \mathrm{~mA} / \mathrm{V}^{2}$, and $\lambda=0.01 \mathrm{~V}^{-1}$. Assume $R_{S i}=4 K \Omega$ and $g_{m}=$ $2 k_{n}\left(V_{G S Q}-V_{T N}\right)$


Figure 5.1

