UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE & ENGINEERING

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS II

COURSE CODE - EE324

MAIN EXAMINATION

MAY 2016

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. There are FOUR questions in this paper. Answer all the questions.

3. Show all your steps clearly in any calculations/work.

4. State clearly any assumptions made.

5. Start each new question on a fresh page.

6. Make sure that this exam contains 3 pages including this one.

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QUESTION ONE (*25 marks*)

a. With the help of block diagrams, define RAM and ROM? What is the difference between PLA and PAL? [8]

b. A 16K × 4 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.

   (i) What is the size of each decoder and how many AND gates are required for decoding the address? [10]

   (ii) Determine the X and Y selections lines that are enabled when the input address is the binary equivalent of 4,000. [7]

QUESTION TWO (*25 marks*)

a. Explain in detail how Hamming code is used for error detection and correction. [10]

b. Obtain the 15-bit Hamming code word for the 11-bit data word 11001101011. [10]

c. Given the above 11-bit data word, generate the composite word for the Hamming code that corrects single errors and detects double errors. [5]

QUESTION THREE (*20 marks*)

Consider the following four functions F1, F2, F3, and F4 of the inputs x, y and z.

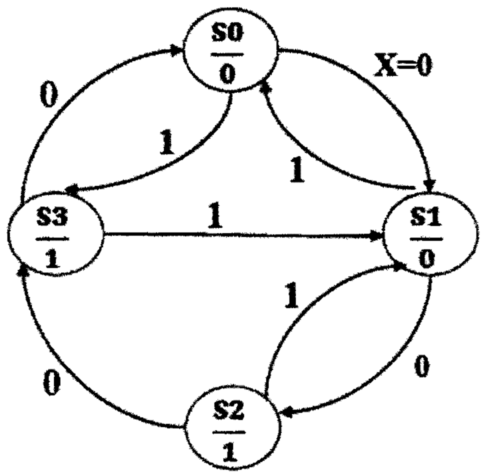
$$F1(x,y,z) = \sum(1,2,5)$$
$$F2(x,y,z) = \sum(2,3,5,7)$$
$$F3(x,y,z) = \sum(1,2,3,5,6,7)$$
$$F4(x,y,z) = \sum(1,3,5,7)$$

a. Tabulate the read-only memory (ROM) truth table and Implement the four functions above using the ROM. [10]

b. Implement the four functions above using the programmable array logic (PAL). NOTE: please write the product term at the output of each AND gate. [10]

QUESTION FOUR *(30 marks)*

Complete the design for the state machine described in the state diagram below.



a. Write out the state table. Assign states using a simple binary order (S0=AB= 00). The write out the transition table. [8]

b. Write out the flip-flop input excitation table assuming JK flip-flops are used. (Note that $Q^+ = J \cdot Q' + K' \cdot Q$.) [10]

c. Draw the circuit diagram. [8]

d. What is the difference between Moore machines and Mealy machines? Is the above circuit Moore or Mealy machine? [4]

JK Flip Flop characteristic Tables		
J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'