UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2015

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE DESIGN III

COURSE CODE: EE421

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

Consider the BJT amplifier shown in Figure-Q1.

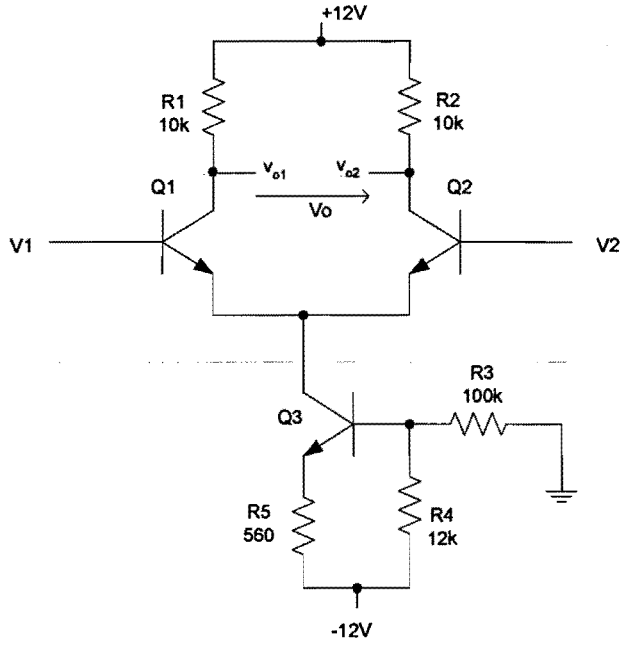

Figure - Q1

(a) Under no input signal, calculate the collector voltage of Q_1 and Q_2, and also emitter and base voltage of Q_3. You may assume that the gains of the transistors are high. (6 marks)

(b) (i) Draw the common mode half circuits and derive an expression for the common mode gain for a single ended output, assuming that the impedance offered by the current source is R_o. (5 marks)

(ii) Calculate the common mode gain in (i) above. (5 marks)

(iii) What is the common mode gain if the output is taken differentially? Calculate this value if R_1 and R_2 are having a tolerance of $\pm 1\%$. (5 marks)

(iv) Find an expression for the common mode input impedance and calculate its value. (4 marks)

Note: (i) Output impedance of the current source $\approx r_o\left[1+\frac{R_E}{\frac{R_E+R_B}{\beta}+r_e}\right]$, in terms of usual notation.

(ii) Assume that the $\beta = 100$, $V_A = 80V$ and $r_\mu = \infty$, unless otherwise stated.

QUESTION TWO *(25 marks)*

In the NMOS amplifier shown in Figure-Q2, the devices Q_1 and Q_2 are matched.

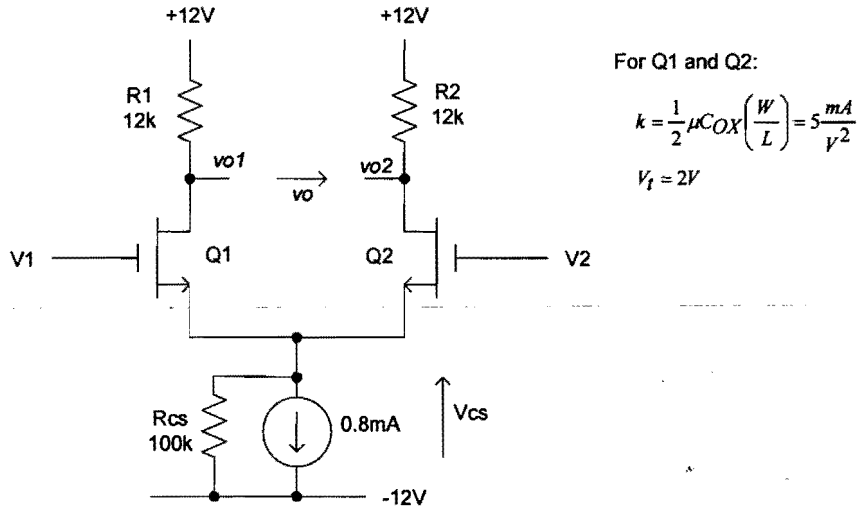

Figure - Q2

(a) Calculate the value of the differential input voltage $V_1 - V_2$, which will result $I_{D2} = 0.6mA$. (4 marks)

(b) A differential input signal v_d is applied to the amplifier. Draw the differential half circuits for mid band signals and calculate the differential gains $\frac{v_{o1}}{v_d}$, $\frac{v_{o2}}{v_d}$ and $\frac{v_o}{v_d}$ proving any formula you use. (8 marks)

(c) Calculate the maximum input common mode voltage range if the voltage drop across the current source is $V_{cs} \geq 3V$. (6 marks)

(d) (i) Find the value of input offset voltage of the amplifier using the data given below.

Tolerance of R_1 and R_2 $= \pm 2\%$

Tolerance of $\frac{W}{L}$ ratio $= \pm 4\%$

Tolerance of V_t $= \pm 0.2\%$ (4 marks)

(ii) Estimate the output dc voltage V_o when the inputs $V_1 = V_2 = 0$ if the tolerances given in d(i) are applicable. (3 marks)

QUESTION THREE *(25 marks)*

(a) A cascode NMOS amplifier is shown in Figure-Q3, in which the transistors Q_1 and Q_2 are matched.

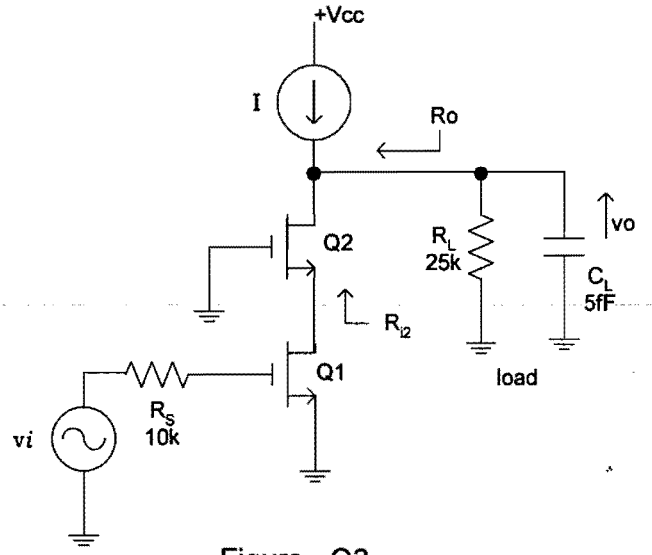

Figure - Q3

Assume the following data of the devices given with usual notation.

$g_m = 1.35\frac{mA}{V}$ $\chi = 0.2$ $r_o = 25k$ $C_{gs} = 18fF$ $C_{gd} = 4fF$ $C_{db} = 5fF$

(a) Show that the output impedance R_o is given by, $R_o = r_{o1} + r_{o2} + r_{o1}r_{o2}(g_{m2} + g_{mb2})$.

(6 marks)

(b) Derive an expression for the mid-band gain $\frac{v_o}{v_i}$ and calculate its value.

(7 marks)

(c) Finding the Miller's components or otherwise, calculate the upper cutoff frequency f_H.

(9 marks)

(d) Calculate the unity gain frequency f_T of the amplifier.

(3 marks)

Note: You may use, $R_{i2} = \frac{R_L + r_{o2}}{1 + r_{o2}g_{m2}}$

QUESTION FOUR (*25 marks*)

(a) Consider the IC amplifier shown in Figure-Q4(a), with the following data.

$K_1 = 5\frac{mA}{V^2}$ $K_2 = 3\frac{mA}{V^2}$ $K_3 = 2\frac{mA}{V^2}$ $|V_t| = 1.5V$
$|V_A| = 70V$ $I_{ref} = 0.8mA$

(i) Calculate the value of R and the bias current of Q_3.

(4 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_i}$ and calculate its value.

(5 marks)

(iii) Estimate the maximum peak to peak value of the output signal at v_o, which can be obtained without any distortion.

(4 marks)

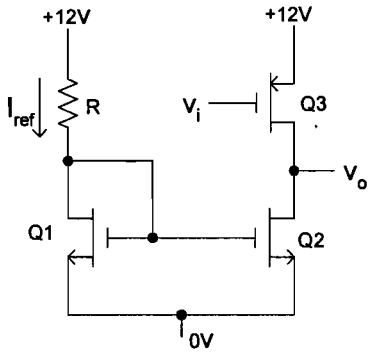

Figure - Q4(a)

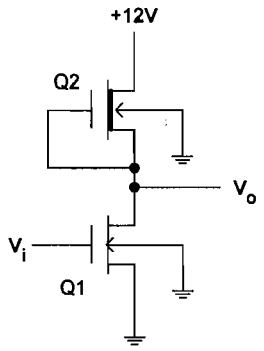

Figure - Q4(b)

(b) In Figure-Q4(b), the devices Q_1 and Q_2 are enhancement and depletion type respectively. You may assume the data given below.

$W_1 = 80\mu m$ $L_1 = 5\mu m$ $W_2 = 5\mu m$ $L_2 = 25\mu m$ $V_{tE} = 1V$
$V_{tD} = -2V$ $\mu C_{OX} = 150\frac{\mu A}{V^2}$ $|V_A| = 50V$ $\chi = 0.2$

(i) Calculate the drain current of Q_1 at no signal.

(4 marks)

(ii) Draw the small signal equivalent circuit considering the body effect and the output resistance. Hence derive an expression for the voltage gain $\left(\frac{v_o}{v_i}\right)$ and calculate its value.

(8 marks)

QUESTION FIVE (25 *marks*)

(a) A circuit of a dc voltage regulator using a NPN Darlington pass transistor is shown in Figure-Q5(a).

(i) Calculate the output voltage. (3 marks)

(ii) Estimate the minimum value of V_{in} that can be used with the regulator. (6 marks)

(iii) If the load current is $1A$, calculate the power dissipation in the pass transistor for the case in (ii) above. (4 marks)

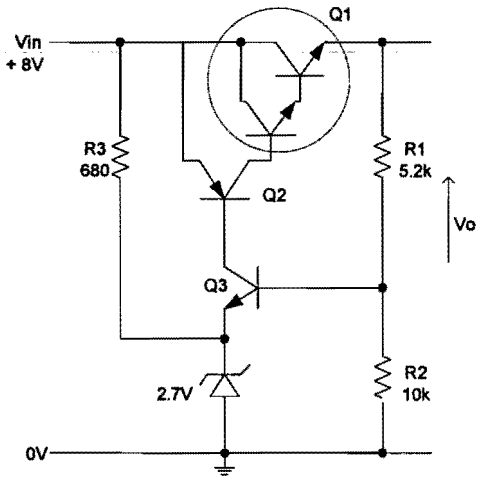

Figure - Q5(a)

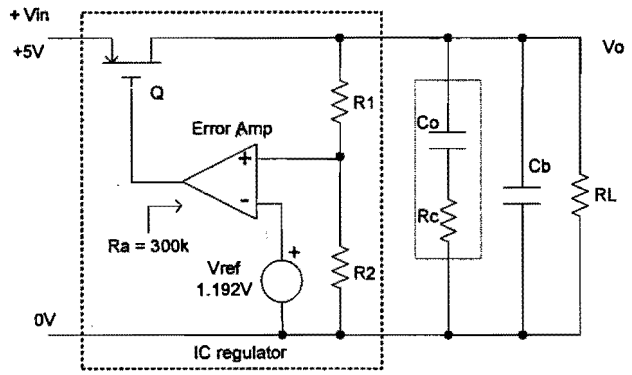

Figure - Q5(b)

(b) The Figure-Q5(b) is a simplified circuit showing an IC regulator connected with a load resistance of R_L associated with a load capacitance of C_b. The output capacitor of the regulator is shown as C_o, with its series equivalent resistance R_C. You may assume the following data.

$C_o = 10\mu F$ $R_C = 2\Omega$ $C_b = 0.5\mu F$ $R_L = 33\Omega$

$r_{ds(Q)} = 65\Omega$ $c_{gs(Q)} = 200pF$

(i) Find the ratio of $\frac{R_1}{R_2}$, for an output voltage $V_o = 3.3V$. (3 marks)

(ii) If the resistances R_1 and R_2 are much larger than the R_L, R_C and $r_{ds(Q)}$, investigate the stability of the circuit, clearly showing the steps followed. The unity gain crossover frequency of the loop gain is $14kHz$. (9 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.