# UNIVERSITY OF SWAZILAND

## SUPPLIMENTERY EXAMINATION

## JULY 2016

## FACULTY OF SCIENCE AND ENGINEERING

## DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE DESIGN III

COURSE CODE: EE421

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

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**QUESTION ONE *(25 marks)***

A differential amplifier using BJTs, is shown in Figure-Q1.

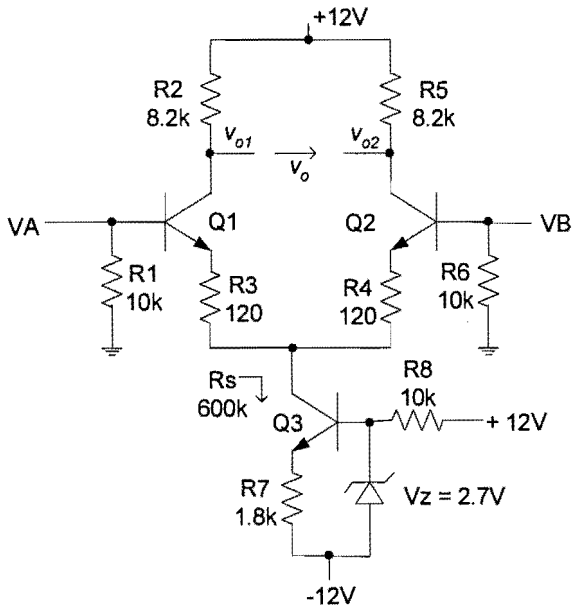



Figure-Q1

(a) Calculate the collector current and collector voltage of each transistor at no signal. Assume that the transistors are of high gain type and matched.

(6 marks)

(b) A signal source $v_d$ is differentially connected to the inputs, such that $v_d = v_A - v_B$. Draw the differential half circuits for the mid-band signals and find the voltage gains $\frac{v_{o1}}{v_d}$, $\frac{v_{o2}}{v_d}$ and $\frac{v_o}{v_d}$, deriving any formula you use.

(8 marks)

(c) Calculate the differential input resistance of the amplifier, assuming $\beta_{Q1} = \beta_{Q2} = 100$.

(5 marks)

(d) If $V_A = V_B = 0$, find the value of $|V_o|$, assuming the following data.

Tolerance of $R_2$ and $R_5 = \pm 5\%$

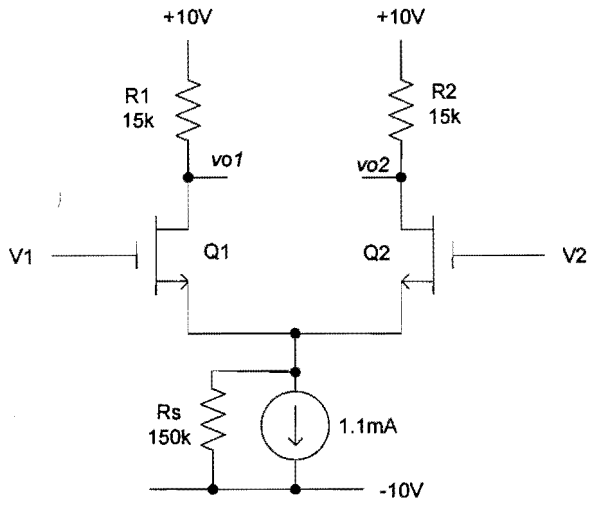
Tolerance of scale current = $\pm 10\%$

You may neglect the tolerances related to other components.

(6 marks)

**QUESTION TWO *(25 marks)***

Consider the NMOS amplifier shown in Figure-Q2. The devices $Q_1$ and $Q_2$ are matched.




For Q1 and Q2:

$$k = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right) = 7\frac{mA}{V^2}$$

$$V_t = 3V$$

Figure - Q2

(a) When a differential voltage $V_D$ is applied to the input, the value of $I_{D2} = 1.1mA$. Find the value of $V_D$, if $V_D = V_1 - V_2$. You may assume standard notation.

(5 marks)

(b) Draw the common mode half circuit for a single ended output. Assuming $V_1 = V_2$, calculate the common mode gain for a single ended output proving any formula you used.

(8 marks)

(c) Calculate the CMRR in dB for the part (b) above.

(7 marks)

(d) Find the numerical value of the common mode gain when the outputs are taken differentially, with the tolerances of resistors being $\pm 5\%$.

(5 marks)

**QUESTION THREE *(25 marks)***

(a) A circuit of a current source implemented with BJTs is shown in Figure-Q3(a), where the devices are matched and of high gain type.

(i) Show that $I_o = I_{ref}\, e^{-\frac{I_o R}{V_T}}$, assuming standard notation

(6 marks)

(ii) Find the component values if the output current is $200\mu A$. You may use the following data.

$V_{CC} = 12V$ $V_{BE1} = 0.6V$ $I_{ref} = 1.2mA$

(6 marks)

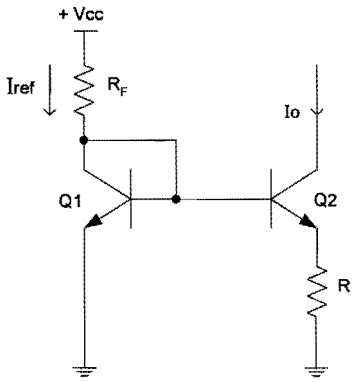



Figure - Q3(a)

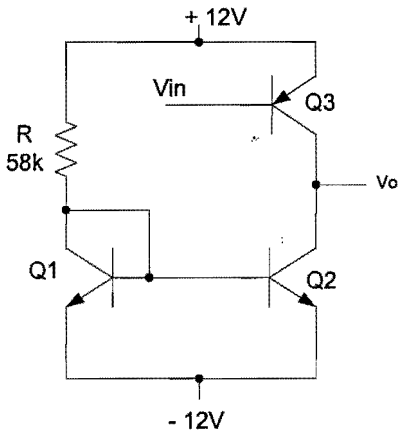



Figure-Q3 (b)

(b) An IC amplifier is shown in Figure-Q3(b). The transistors are of high gain type while $Q_1$ and $Q_2$ are matched.

(i) Find the emitter current of $Q_3$. (4 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value. Assume that the $V_A = 75V$. (5 marks)

(iii) What is the voltage gain if this amplifier drives an external load of $25k$ connected to the output through a large capacitor? (4 marks)

**QUESTION FOUR (*25 marks*)**

(a) An amplifier implemented in CMOS technology is shown in Figure-Q4(a), having the following data.

$K_1 = 8\frac{mA}{V^2}$ $K_2 = 4\frac{mA}{V^2}$ $K_3 = 6\frac{mA}{V^2}$

$|V_t| = 2V$ $|V_A| = 60V$

(i) Calculate the bias voltage $V_i$ required at the input. (4 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_i}$ and calculate its value. (5 marks)

(iii) Determine the maximum and minimum signal limits of $v_0$. (4 marks)

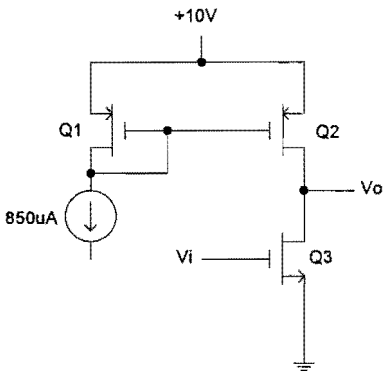



Figure-Q4(a)

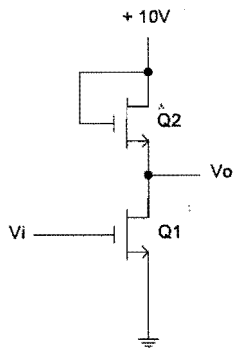



Figure-Q4(b)

(b) An enhancement type NMOS amplifier is shown in Figure-Q4(b). You may assume the following data with respect to this circuit.

$L_1 = 10\mu m$ $L_2 = 20\mu m$ $W_1 = 800\mu m$ $W_2 = 10\mu m$

$V_t = 2V$ $\mu C_{OX} = 200\frac{\mu A}{V^2}$ $V_A = 80V$

(i) Find the dc voltage to be applied at the input, such that the value of $V_o = 6V$. What is the current flowing in $Q_2$? (6 marks)

(ii) Draw the ac equivalent circuit for mid-band signals and hence calculate the mid band voltage gain. (6 marks)

**QUESTION FIVE (25 *marks*)**

A cascode amplifier is shown in Figure-Q5.

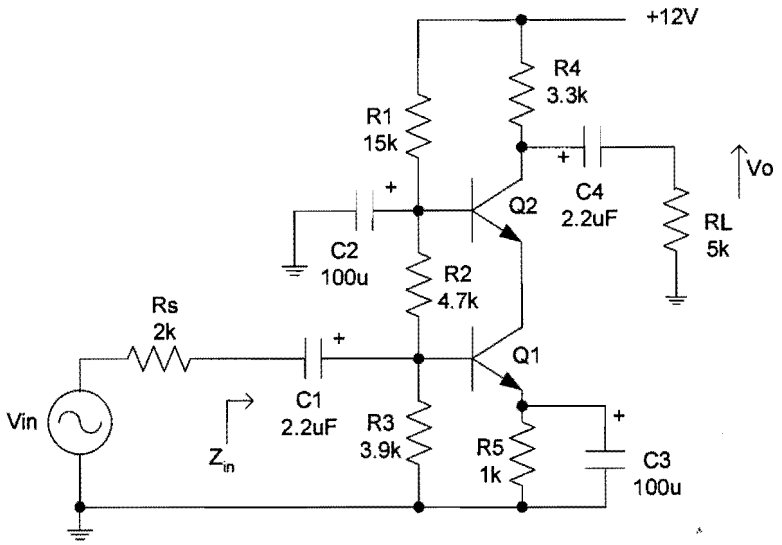



Figure-Q5

(i) Find the voltages at the terminals of two transistors under no signal. You may assume that the transistors are identical and of high gain type.

(8 marks)

(ii) Derive an expression for the mid-band gain $\frac{v_o}{v_{in}}$, and find its value. Assume that the $\beta = 100$ and the Early effect is negligible.

(11 marks)

(iii) Find an expression with numerical values, for the input impedance $Z_{in}(\omega)$ at high frequency signals.

(6 marks)

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## 1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

## 2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.