UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE & ENGINEERING

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS I

COURSE CODE - EE322

MAIN EXAMINATION

DECEMBER 2016

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

1. There are FIVE questions in this paper. Answer any FOUR questions.
2. Each question caries 25 marks.
3. Show all your steps clearly in any calculations/work.
4. Start each new question on a fresh page.

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QUESTION ONE (*25 marks*)

(a) (9 pts) Complete the following table of equivalent values.

Binary	Octal	Decimal	Hexadecimal
	13.14		
			1D.FD
11011.010011			

(b) (6 pts) Perform subtraction on the following unsigned binary numbers using 2's complement of the subtrahend.

(i) $101010 - 101011$

(ii) $1011 - 110000$

(c) (10 pts) Using postulates and theorems of Boolean algebra, reduce the combinational circuit shown in figure below to a minimum number of literals. Draw the circuit using one gate.
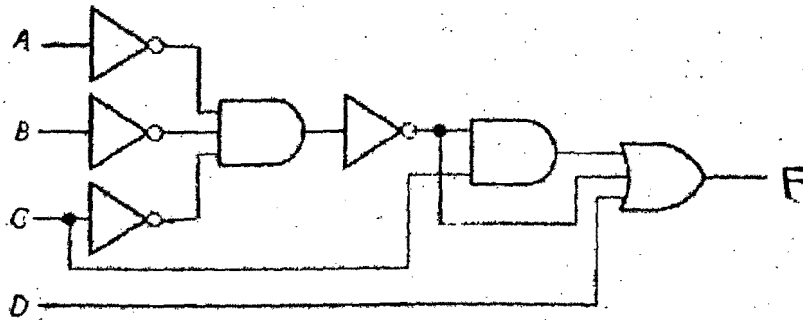
QUESTION TWO (*25 marks*)

a)   (6 pts) Simplify the following using a k-map:

$$F(A, B, C, D) = \Sigma(1, 3, 5, 7, 9)$$
$$d(A, B, C, D) = \Sigma(4, 6, 12, 13)$$

b)   (7 pts) Draw a NAND logic diagram that implements the complement of the following function:

$$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 8, 9, 12)$$

c)   (4 pts) Using Boolean algebra simplify the following Boolean expression to a minimum number of literals:
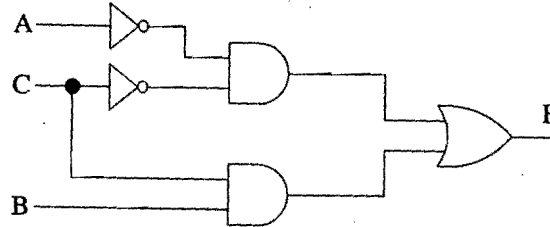
$$F = (x'y' + z)' + z + xy + wz$$

d)   (8 pts) Implement the following Boolean function with a multiplexer:

$$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$$

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QUESTION THREE (25 marks)

(a) (4 pts) Determine the minterm expansion for F(A,B,C) in the diagram below.

(b) (5 pts) Determine the maxterm expansion for $F = xy + x'z$.

(c) (6 pts) Give the Characteristic equations and the Excitation tables for SR and JK flip-flops.

(d) (5 pts) Simplify the following Boolean function using a Karnaugh map.

$$F(w,x,y,z) = xyz + wy + wxy' + x'y$$

(e) (5 pts) Indicate how a NAND gate can be used to implement

   (i)   An inverter:

   (ii)   An AND Gate:

QUESTION FOUR (25 marks)

(a) (15 pts) A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Figure below. The numeric display chosen to represent the decimal digit is also shown below. Design this decoder using a minimum of gates. The six invalid combinations should result in a blank display.

Segment designation   Numerical designation for display
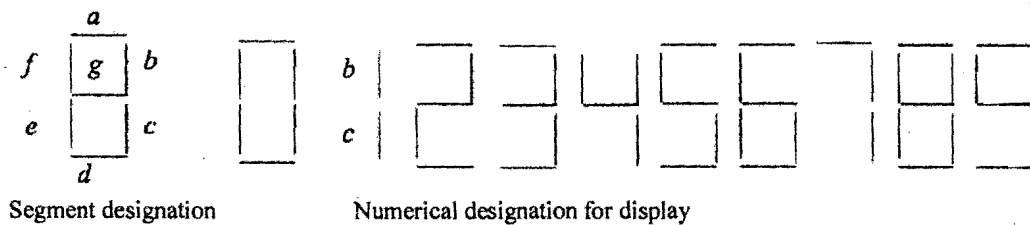
(b) (10 pts) Design a combinational circuit with three inputs and one output. The output is one when the binary value of the inputs is less than 3. The output is 0 otherwise.

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QUESTION FIVE (*25 marks*)

a) (10 pts) A combinational circuit is defined by the following three Boolean functions:

$$F_1 = x'y'z' + xz$$
$$F_2 = xy'z' + x'y$$
$$F_3 = x'y'z + xy$$

Design the circuit with a decoder and external gates.

b) (15 pts) A sequential circuit has two JK flip-flops A and B. two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are:

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$

$$J_B = A'x + X'A \qquad K_B = A + xy'$$

$$Z = Ax'y' + Bx'y'$$

(i)   Sketch the logic diagram of the circuit.

(ii)   Tabulate the state table.

(iii) Derive the state equations for A and B.