UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2016

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

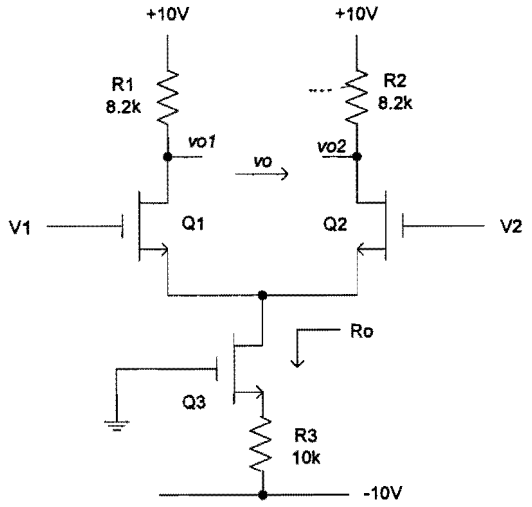
1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

Consider the NMOS differential amplifier shown in Figure-Q1. The devices Q_1 and Q_2 are matched.



For Q1 and Q2:

$$k = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right) = 6\frac{mA}{V^2}$$
$$V_t = 1V$$

For Q3:

$$k = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right) = 4\frac{mA}{V^2}$$
$$V_t = 1V$$

Figure - Q1

(a) Calculate the drain current of each device at no input signal and hence calculate the drain voltages of Q_1 and Q_2. (7 marks)

(b) If $V_1 = V_2 = 5V$ is maintained as the dc bias voltage, find the drain voltage of Q_3. (3 marks)

(c) Draw the common mode half circuits and derive an expression for the common mode gain with respect to a single output. (4 marks)

(d) Calculate the common mode gain in (c) in dB. (6 marks)

(e) What is the common mode gain over the output denoted by v_o? Find its value in dB if R_1 and R_2 are having a tolerance of $\pm 2\%$. (5 marks)

Note: You may assume that,

(i) the output impedance of the current source $\approx [r_o + R_s + g_m r_o R_s]$, and

(ii) $V_A = 50V$, in terms of usual notation.

QUESTION TWO *(25 marks)*

Consider the BJT cascode amplifier shown in Figure-Q2.

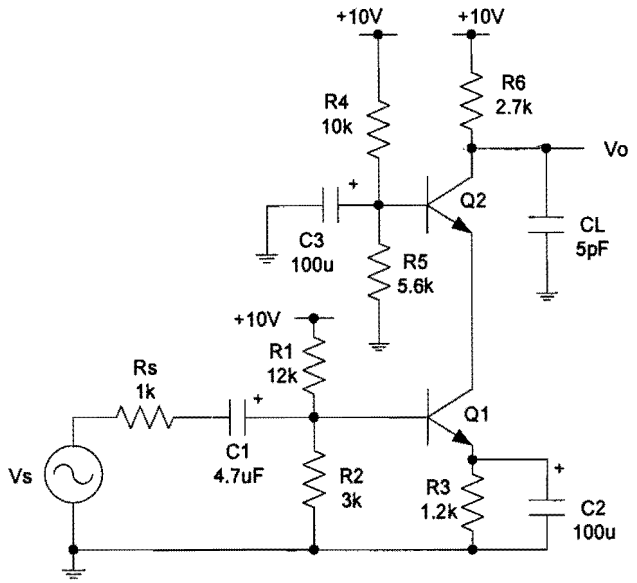


Figure-Q2

(a) Assuming that the transistors are identical and of high gain type, find the collector currents and collector voltage of each transistor.

(6 marks)

(b) You may use the parameters of the devices $Q_1$and Q_2, which are given below with usual notation.

$\beta = 100 \qquad C_\pi = 16pF \qquad C_\mu = 4pF \qquad r_o = \gg$

(i) Derive an expression for the mid-band gain $\frac{v_o}{v_s}$ and calculate its value.

(7 marks)

(ii) Calculate the upper cut off frequency f_H using the Miller's components.

(9 marks)

(iii) Find the unity gain crossover frequency f_T of the amplifier.

(3 marks)

QUESTION FOUR (*25 marks*)

(a) In the IC amplifier shown in Figure-Q4(a), the transistors are of high gain and matched. Assuming that the $V_A = 100V, \beta = 100$ for all transistors, find

(i) the collector current of Q_2 at no signal.

(2 marks)

(ii) an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value.

(7 marks)

(iii) the input impedance R_{in} and the output impedance R_o.

(4 marks)

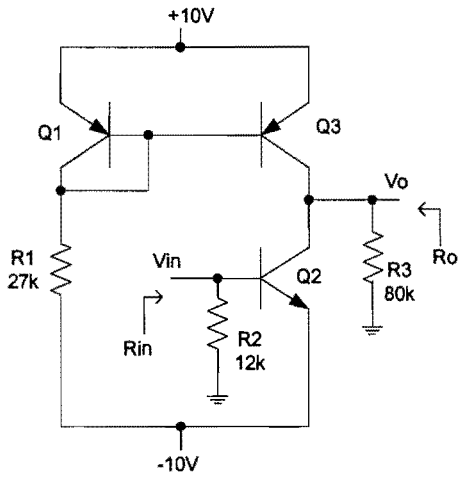


Figure-Q4(a)

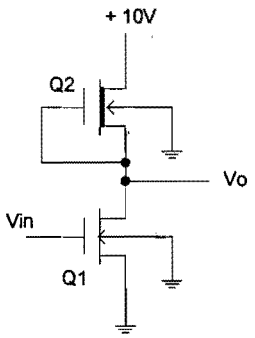


Figure-Q4(b)

(b) Consider the MOS amplifier shown in Figure-Q4(b). The devices Q_1 and Q_2 are of enhancement type and depletion type respectively. You may assume the following data.

$W_1 = 150\mu m$ $L_1 = 5\mu m$ $W_2 = 10\mu m$ $L_2 = 40\mu m$ $V_{tE} = 2V$
$V_{tD} = -3V$ $\mu C_{OX} = 100\frac{\mu A}{V^2}$ $|V_A| = 80V$ $X = 0.2$

(i) Find the bias current in Q_1 at no signal.

(4 marks)

(ii) Draw the small signal equivalent circuit including the body effect and the output resistance of the devices. Hence derive the voltage gain $\left(\frac{v_o}{v_i}\right)$ and find its value. The input biasing scheme is omitted for simplicity.

(8 marks)

QUESTION FIVE (25 *marks*)

A circuit of a linear voltage regulator is shown in Figure-Q5.

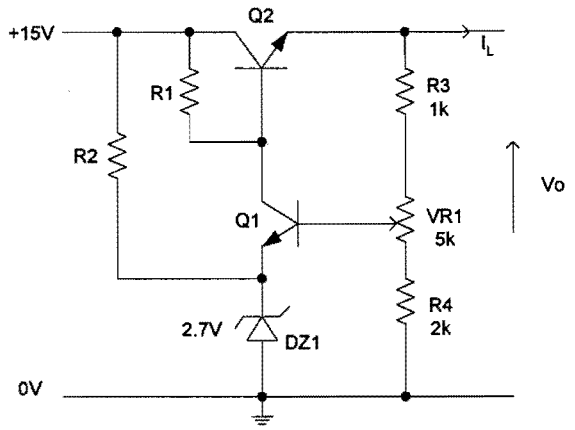


Figure-Q5

(a) Calculate the minimum and maximum output voltage.

(4 marks)

(b) Find the guaranteed maximum output current specification if the maximum allowable power dissipation of Q_2 is $25W$.

(4 marks)

(c) Calculate the values of R_1 and R_2 and then select resistors from E12 range using the following data. You may assume usual notation.

$\beta_{Q2} = 25$ $I_{C1}(minimum) = 6mA$

$I_Z(minimum) = 8mA$ $I_L(max) = 2A$

(6 marks)

(d) Design an active current limit circuit for this regulator, which will limit the output current to $2A$. Draw your circuit showing the component values.

(5 marks)

(e) Calculate the expected maximum and minimum efficiency of the regulator circuit in Figure-Q5, at a load current of $2A$.

(6 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.