UNIVERSITY OF SWAZILAND

SUPPLIMENTERY EXAMINATION

JULY 2017

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are four questions in this paper. Answer all FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SIX (6) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

Consider the differential amplifier circuit is shown in Figure-Q1. The transistors are matched and $\beta = 125$.

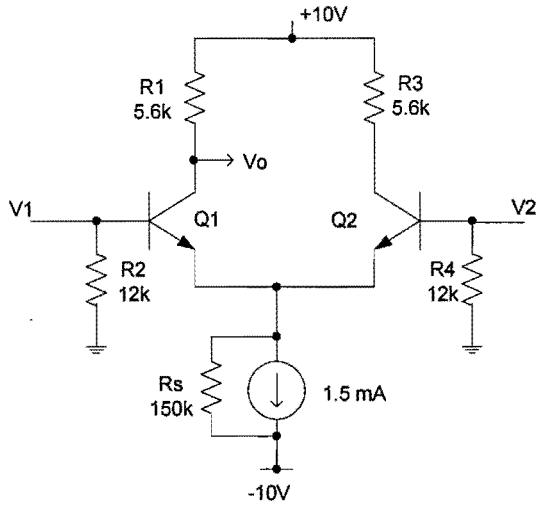

Figure-Q1

(a) Under quiescent conditions, calculate the collector voltage and the base voltage of Q_1.

(8 marks)

(b) Draw the differential half circuit for ac signals. Derive an expression for the differential voltage gain $\frac{v_o}{v_d}$ and calculate its value. Assume that $v_d = (v_1 - v_2)$.

(8 marks)

(c) Find the common mode gain at the output v_o deriving any formula you use. Hence calculate the CMRR in dB.

(9 marks)

QUESTION TWO *(25 marks)*

(a) In the Widlar current source shown in Figure-Q2(a), the transistors Q_1 and Q_2 are matched and of high gain type.

(i) Find a relationship between I_o and I_{ref}.

(4 marks)

(ii) If the power supply used is $10V$, show how you are going to implement this current source for $I_o = 125\mu A$. Assume that for the given transistors, when the $V_{BE} = 0.62V$, the $I_C = 0.73mA$.

(5 marks)

(iii) Calculate the output resistance R_o, if the $V_A = 80V$ and the $\beta = 100$.

(4 marks)

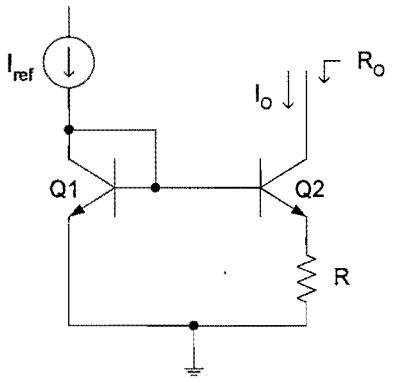

Figure-Q2(a)

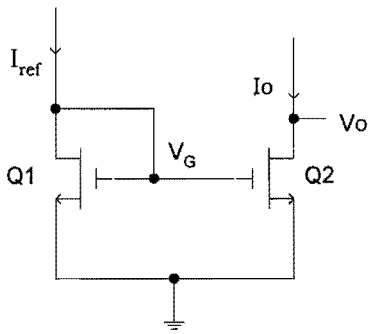

Figure-Q2(b)

(b) Consider the current mirror shown in Figure-Q2(b). Some of the process parameters of the devices are given below.

$L_1 = L_2 = 5\mu m$ $W_1 = 25\mu m$ $W_2 = 50\mu m$ $V_t = 2V$

$\mu C_{ox} = 60\frac{\mu A}{V^2}$ $V_A = 80V$ $I_o = 150\mu A$

(i) Find the voltage V_G.

(4 marks)

(ii) Calculate the value of I_{ref}.

(4 marks)

(iii) If $V_o = 12V$, estimate the output current for the case (ii) above.

(4 marks)

QUESTION THREE ***(25 marks)***

(a) Consider the IC amplifier shown in Figure-Q3(a). Assume that the transistors are of high gain and matched. You may assume that the $V_A = 80V$ and $\beta = 125$. Find,

(i) the collector current of Q_3.

(2 marks)

(ii) an expression for the voltage gain $\frac{v_o}{v_S}$ and calculate its value.

(7 marks)

(iii) the input impedance R_{in} and the output impedance R_o.

(3 marks)

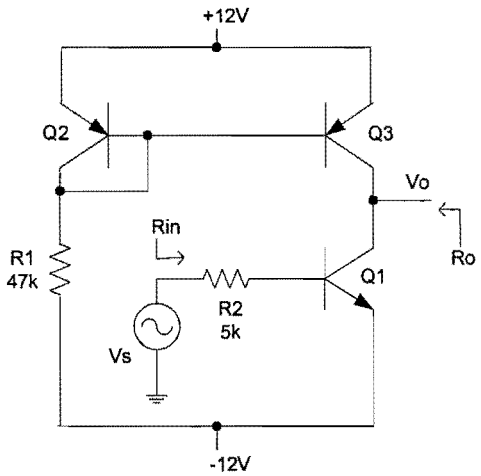

Figure-Q3(a)

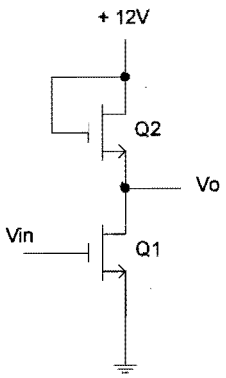

Figure-Q3(b)

(b) An enhancement type NMOS amplifier is shown in Figure-Q3(b). Some useful parameters of the devices used are,

$W_1 = 120\mu m$ $W_2 = 10\mu m$ $V_t = 1V$ $\mu C_{OX} = 200\frac{\mu A}{V^2}$

$L_1 = 10\mu m$ $L_2 = 50\mu m$

(i) Find the drain current of Q_2 if a dc voltage of $1.6V$ is applied to v_{in}. Calculate the value of v_o for this case.

(5 marks)

(ii) Draw the small signal equivalent circuit. Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value. Use that $V_A = 80V$.

(8 marks)

QUESTION FOUR (*25 marks*)

Consider the voltage regulator circuit shown in Figure-Q4.

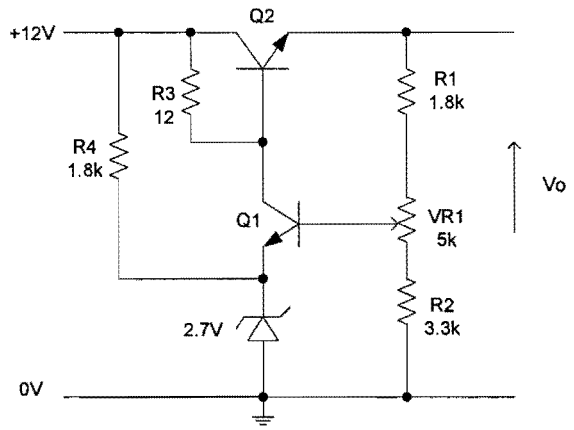

Figure-Q4

(i) Find the minimum and maximum output voltage.

(6 marks)

(ii) If the maximum possible power dissipation of Q_2 is $18W$, find the load current specification of the regulator.

(3 marks)

(iii) Show how you are going to implement an active current limit for a maximum load current of $1.5A$. Give the specifications of the components required.

(5 marks)

(iv) If $\beta_{Q2} = 25$, calculate the maximum possible power dissipation in R_3, R_4 and in the zener diode.

(6 marks)

(v) Estimate the minimum efficiency of the regulator, neglecting any current limit arrangement.

(5 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.