UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE & ENGINEERING

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS II

COURSE CODE – EE324

MAIN EXAMINATION

MAY 2018

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO STUDENTS

1. There are **FOUR** questions in this paper. Answer **ALL** the questions.
2. Each question caries 25 marks.
3. Show all your steps clearly in any calculations/work.
4. Start each new question on a fresh page.
5. Make sure that this exam contains 3 pages including this one.

DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

QUESTION ONE *(25 marks)*

(a) A 4K x 8 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.

(i) What is the size of each decoder and how many AND gates are required for decoding the address [pt. 6] ?

(ii) Determine the X and Y selections lines that are enabled when the input address is the binary equivalent of 2,600 [pt. 4].

(b) Specify the size of a ROM that will accommodate the truth table for the following combinational circuit components [pt. 6].

(i) A binary multiplier that multiplies two 4-bit numbers.

(ii) A 4-bit adder-subtractor.

(iii) A BCD-to-seven-segment decoder with an enable input.

(c)

(i) How many 32K × 8 RAM chips are needed to provide a memory capacity of 256K bytes [pt. 3]?

(ii) How many address lines and input-output data lines are needed for a 2G × 32 RAM [pt. 3]?

(iii) What are the advantages of dynamic RAM over static RAM [pt. 3]?

QUESTION TWO *(25 marks)*

(a) What is the difference between PLA and PAL [pt. 2]?

(b) Tabulate the truth table for an 8 × 4 ROM that implements the Boolean functions

$$A(x,y,z) = \sum(1,2,5,6)$$
$$B(x,y,z) = \sum(0,1,6,7)$$
$$C(x,y,z) = \sum(2,6)$$
$$D(x,y,z) = \sum(1,2,3,5,6,7)$$

Considering the ROM as a memory, specify the memory contents at addresses 3 and 6 [pt. 5].

(c) Implement the four functions above (b) using the PLA programming. Minimize the number of product terms [pt. 10].

(d) Obtain the 15-bit Hamming code word for the 11-bit data word 11001101011 [pt. 8].

QUESTION THREE (*25 marks*)

(a) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. Determine the original 8-bit data word that was written into memory if the 12-bit word read out is 101110000110 [pt. 5].

(b) A sequential circuit has 2 edge triggered flip-flops (outputs A and B), two inputs (X and Y) and one output Z. The logic expressions for this circuit are [pt. 20]:

$$D_a = X' \cdot Y + X \cdot A$$
$$J_b = X' \cdot B + X' \cdot A$$
$$K_b = Y \cdot B$$
$$Z = X \cdot B$$

(i) Construct a transition table (first, construct the flip-flop excitation table.)

(ii) Construct a state diagram

QUESTION FOUR (*25 marks*)

(a) Briefly describe the basic building blocks of Algorithmic State Machine (ASM) chart [pt. 5].

(b) Draw an ASM chart and state diagram to describe a sequence detector that detects a sequence of 101 [pt. 20].