UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2017

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: ANALOGUE DESIGN III

COURSE CODE: EE421

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

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THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

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QUESTION ONE (25 marks)

A circuit of a differential amplifier is shown in Figure-Q1.

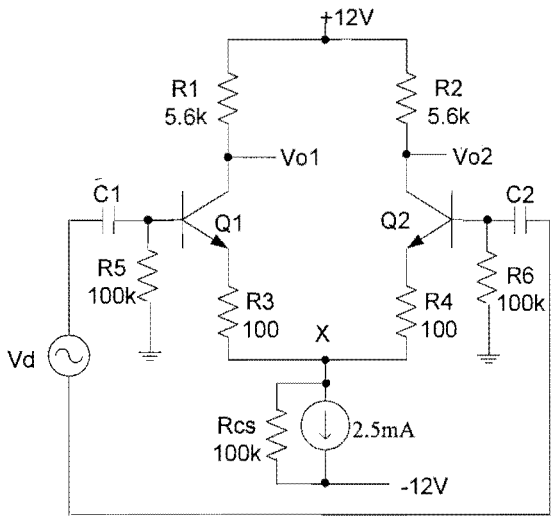

Figure-Q1

You may assume that Q_1 , $Q_2$are of matched high gain type and C_1 , C_2 are large unless stated otherwise.

(a) Find the voltage at the collector of $Q_1$and at X when no input signal is applied.

(4 marks)

(b) Draw the differential half circuits. Hence calculate the differential voltage gains $\frac{v_{02}}{v_d}$ and $\frac{v_{02}-v_{01}}{v_d}$, deriving any formula you use.

(7 marks)

(c) Draw the common mode half circuit for Q_2. Derive an expression for the common mode gain at the output v_{02}, calculate its value and find the $CMRR$ in dB.

(7 marks)

(d) If $R_3 = R_4 = 0$, estimate the high frequency $3dB$ bandwidth.

$C_\pi = 14pF$ $C_\mu = 2pF$ $r_o = \infty$ $\beta = 100$

(7 marks)

QUESTION TWO ***(25 marks)***

(a) Consider the circuit shown in Figure-Q2(a) where the two transistors Q_1 and Q_2 are matched.

(i) If β is the current gain of the transistors, find an expression for I_o with I_{ref}.

(3 marks)

(ii) Calculate the value of R that will give $I_o = 1mA$, assuming a β of 50.

(4 marks)

(iii) Calculate the output resistance R_o when I_o is $1mA$. Hence find the value of output current I_o when the output voltage v_o is $5V$. Assume that the $V_A = 100V$.

(7 marks)

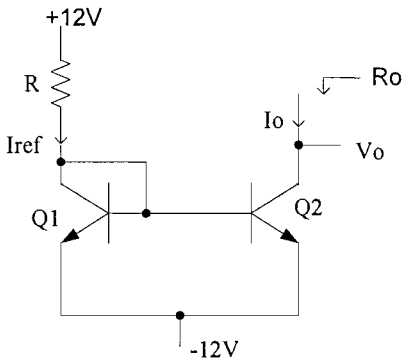

Figure-Q2(a)

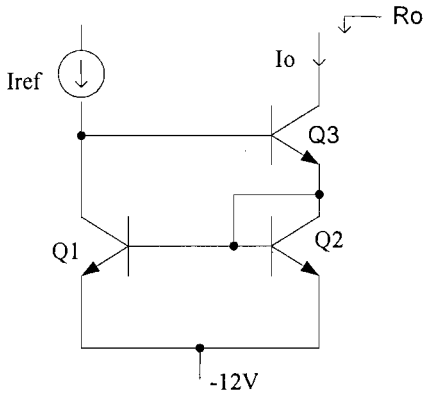

Figure-Q2(b)

(b) A circuit of a current source with matched transistors are shown in Figure-Q2(b).

(i) State two advantages of this circuit.

(2 marks)

(ii) Derive an expression for the output current I_o.

(6 marks)

(iii) Estimate the value of R_o. You may use any formula known to you.

$I_{ref} = 150\mu A$ $V_A = 80V$ $\beta = 100$

(3 marks)

QUESTION THREE *(25 marks)*

(a) An IC amplifier using enhancement type NMOS devices is shown in Figure-Q3(a).

(i) Under quiescent conditions, derive an expression for V_o in terms of V_{in}.

(6 marks)

(ii) Calculate the value of V_o when $V_{in} = 1.5V$, under no signal conditions. You may also assume,

$W_1 = 160\mu m$ $L_1 = 10\mu m$ $W_2 = 10\mu m$ $L_2 = 60\mu m$ $V_t = 1.2V$

(4 marks)

(iii) Draw the small signal equivalent circuit neglecting the body effect. Hence derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and evaluate its value using the device data given in (ii) above. Assume that the values of r_{o1} and r_{o2} are large.

(8 marks)

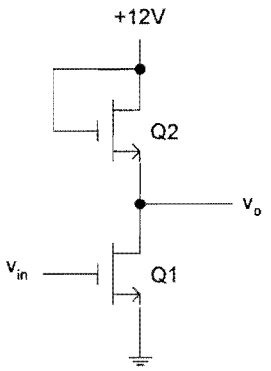

Figure - Q3(a)

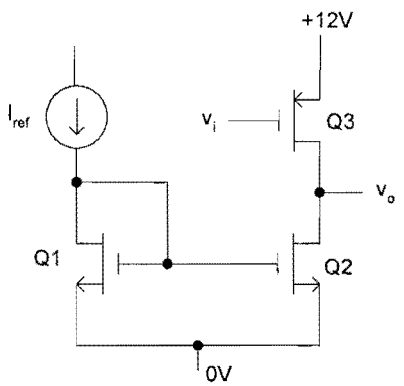

Figure - Q3(b)

(b) The circuit in Figure-Q3(b), shows a CMOS amplifier with the following data. You may assume usual notation.

$K_1 = 5\frac{mA}{V^2}$ $K_2 = 2.5\frac{mA}{V^2}$ $K_3 = 3\frac{mA}{V^2}$ $I_{ref} = 0.8mA$

$|V_t| = 1.2V$ $|V_A| = 80V$

(i) Calculate the source current of Q_3 at no signal.

(3 marks)

(ii) Derive an expression for the voltage gain $\left(\frac{v_o}{v_i}\right)$ and calculate its value.

(4 marks)

QUESTION FOUR (*25 marks*)

A circuit of a cascode amplifier is shown in Figure-Q4.

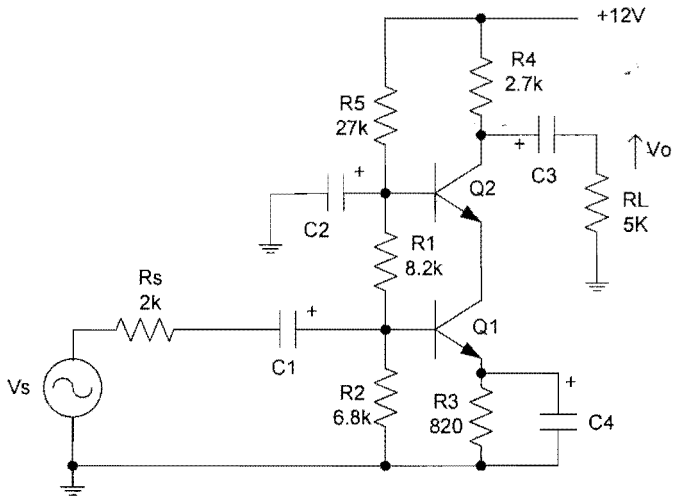

Figure -Q4

Assume that the transistors are identical. The coupling and by-pass capacitors and r_o can be assumed as large.

(a) (i) Calculate the collector current and collector voltage of Q_1 under no signal conditions. You may state any assumptions used.

(4 marks)

(ii) Find an expression for the mid-band gain $\left(\frac{v_o}{v_s}\right)$, assuming usual notation.

(6 marks)

(iii) Calculate the mid-band gain of the amplifier if $\beta = 100$.

(5 marks)

(b) Estimate the values of pole frequencies of the amplifier and hence determine the high frequency 3 dB bandwidth. You may use,

$C_\pi = 13pF$ $C_\mu = 3pF$ $\beta = 100$

(10 marks)

QUESTION FIVE (25 *marks*)

(a) Consider the DC regulator circuit shown in Figure-Q5(a).

(i) Calculate the output voltage range.

(4 marks)

(ii) If the maximum power dissipation in Q_1 is limited to $12W$, find the guaranteed maximum load current.

(6 marks)

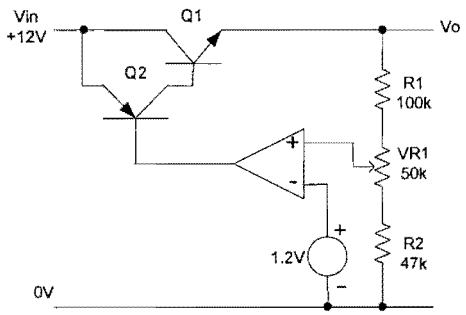

Figure - Q5(a)

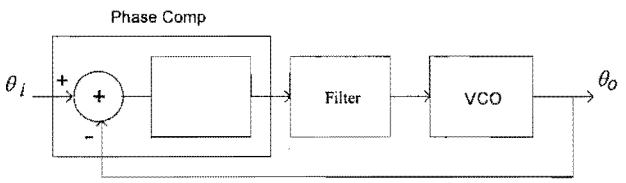

Figure - Q5(b)

(b) A block diagram of a phased locked loop (PLL) is shown in Figure-Q5(b). The phases of the signals are shown as θ_i and θ_o.

(i) Derive the transfer function $\left(\frac{\theta_o}{\theta_i}\right)$ for the system if the filter is a simple RC (single R and single C) network.

(8 marks)

(ii) If the filter components are $0.01\mu F$ and $2.2k$ respectively, estimate the value of σ for the PLL.

$K_P = 4.77\frac{V}{rad}$ $K_V = 1.07 \times 10^3\ \frac{Hz}{V}$

(7 marks)

1. SOME USEFUL MOSFET EQUATIONS

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \text{ in triode region}$$

$$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2 \text{ in saturation region}$$

$$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS}) \text{ in saturation region with Channel Modulation effect}$$

$$V_A = \frac{1}{\lambda}$$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.