UNIVERSITY OF SWAZILAND

SUPPLIMENTERY EXAMINATION

JULY 2018

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE DESIGN III
COURSE CODE:	EE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. **There are four questions in this paper. Answer all FOUR questions. Each question carries 25 marks.**
2. **If you think not enough data has been given in any question you may assume any reasonable values.**
3. **Some useful formulas are given in the last page.**

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THIS PAPER CONTAINS SIX (6) PAGES INCLUDING THIS PAGE

QUESTION ONE (*25 marks*)

Consider the differential amplifier shown in Figure-Q1.

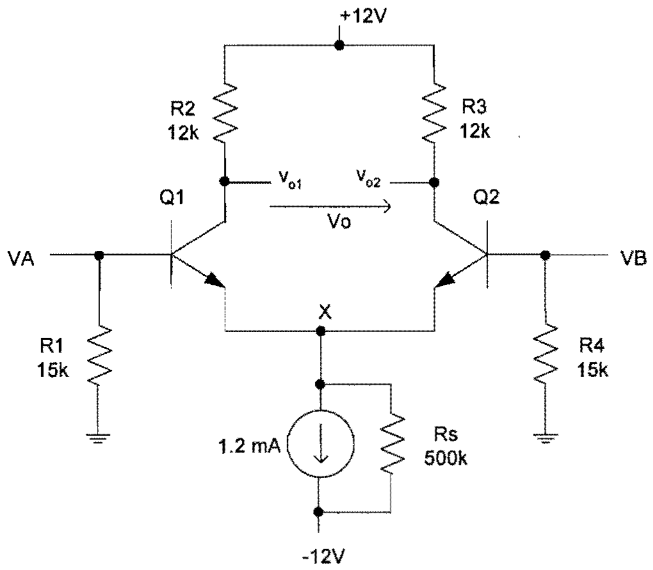

Figure - Q1

(a) Calculate the collector current and collector voltage of each transistor at no signal, assuming that the transistors are of high gain type and matched. What is the voltage at the point $'X'$?

(8 marks)

(b) A voltage source v_d is connected to the inputs such that, $v_d = v_A - v_B$. Draw the differential half circuits for mid-band signals and find the voltage gains $\frac{v_{o1}}{v_d}$, $\frac{v_{o2}}{v_d}$ and $\frac{v_o}{v_d}$, deriving any formula used.

(10 marks)

(c) Find the value of $|V_o|$ when $V_A = V_B = 0$, assuming the following data.

R_2 and R_3 tolerance $= \pm 2\%$

Scale current tolerance $= \pm 20\%$

(7 marks)

QUESTION TWO *(25 marks)*

The amplifier shown in Figure-Q2 uses NMOS transistors, which are matched.

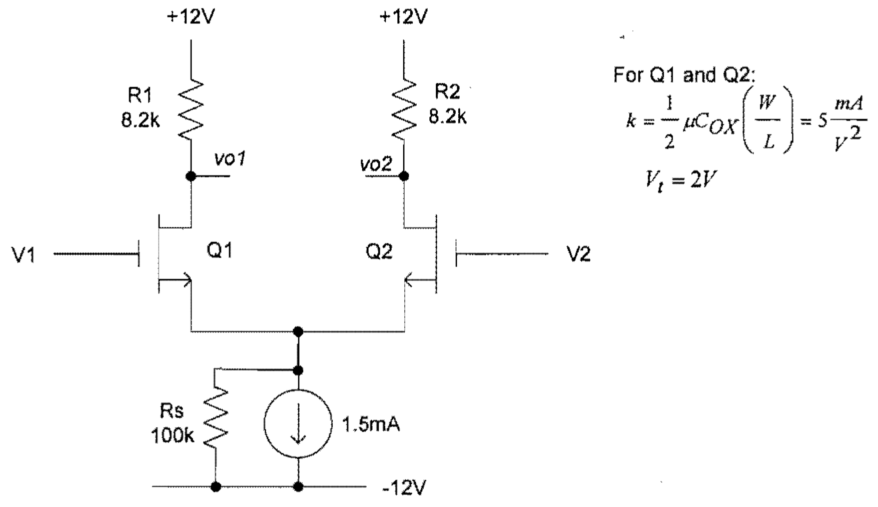

Figure - Q2

(a) Find the value of the differential input voltage V_D given by $V_D = V_1 - V_2$, resulting $I_{D1} = 1.5mA$ assuming standard notation.

(6 marks)

(b) If $V_1 = V_2$, draw the common mode half circuit for a single ended output. Then calculate the common mode gain for a single ended output deriving any formula used.

(12 marks)

(c) Calculate the CMRR in dB for the part (b) above.

(7 marks)

QUESTION THREE *(25 marks)*

(a) An IC amplifier is shown in Figure-Q3(a). The transistors Q_1 and Q_2 are of high gain and matched.

(i) Calculate the emitter current of Q_3.

(3 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value. You may assume that the $V_A = 75V$ and $\beta_{Q3} = 100$.

(7 marks)

(iii) Find the overall voltage gain, if this amplifier is connected to a load of $20k$ through a large capacitor.

(3 marks)

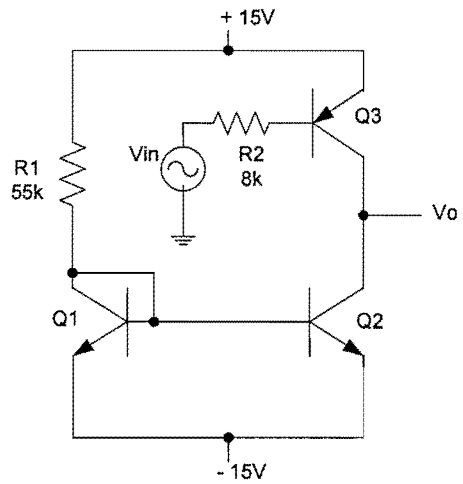

Figure-Q3(a)

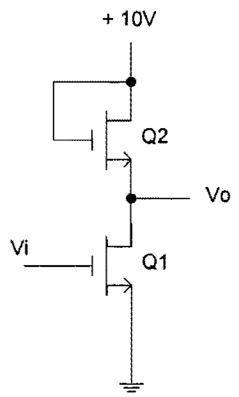

Figure-Q3(b)

(b) An enhancement type NMOS amplifier is shown in Figure-Q3(b). You may assume the following data.

$W_1 = 600\mu m$ $W_2 = 20\mu m$ $V_t = 2V$ $\mu C_{OX} = 250\frac{\mu A}{V^2}$

$L_1 = 10\mu m$ $L_2 = 30\mu m$ $V_A = 75V$

(i) Find the dc voltage to be applied at the input, such that the value of V_o is 5.5V. Also calculate the drain current of Q_2.

(6 marks)

(ii) Draw the ac equivalent circuit for mid-band signals. Hence derive an expression for the voltage gain $\frac{v_o}{v_i}$ and calculate its value.

(6 marks)

QUESTION FOUR (*25 marks*)

A circuit of a voltage regulator is shown in Figure-Q4.

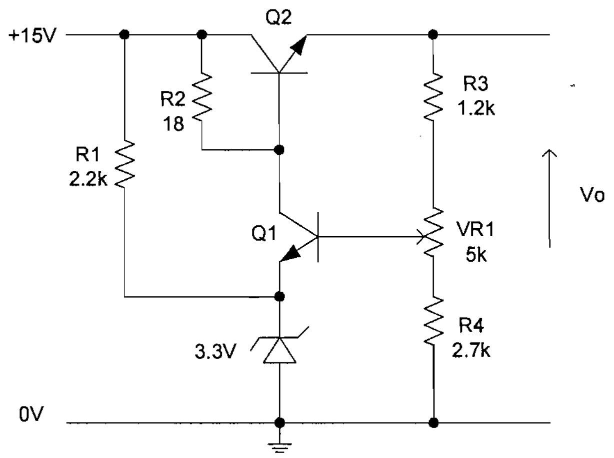

Figure-Q4

(i) Find the range of the output voltage V_o.

(6 marks)

(ii) If the maximum load current is $1.5A$, find the power dissipation rating of Q_2.

(3 marks)

(iii) Find the maximum possible power dissipation in R_1, R_2 and in the zener diode if the current gain of Q_2 is 20.

(6 marks)

(iv) Calculate the minimum efficiency of the regulator.

(5 marks)

(v) Suggest an active overload protection to this circuit showing enough details of the components required.

(5 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. **Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.**