UNIVERSITY OF ESWATINI

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2018

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS II
COURSE CODE:	EEE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

A BJT differential amplifier shown in Figure-Q1 uses matched transistors.

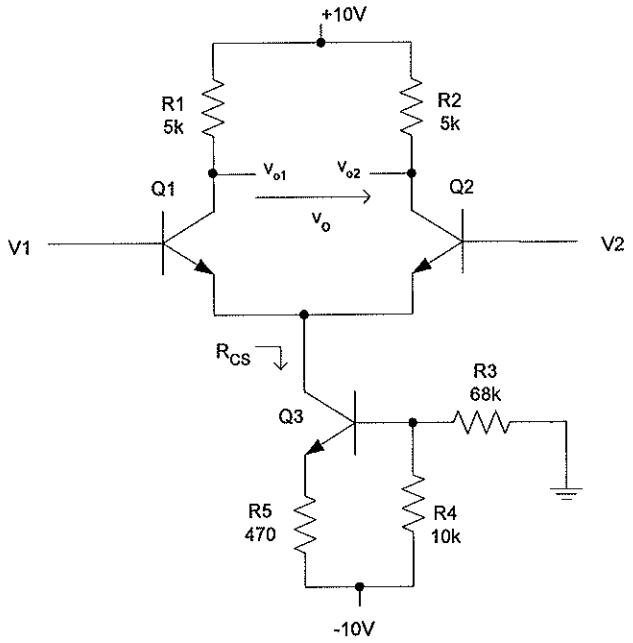

Figure - Q1

(a) Under no input signal, calculate the collector current of Q_3 and the collector voltages of Q_1 and Q_2. You may assume that the gains of the transistors are high.

(6 marks)

(b) (i) Draw the common mode half circuits and derive an expression for the common mode gain for a single ended output.

(5 marks)

(ii) Calculate the common mode gain in (i) above if $R_{CS} = 100k$.

(4 marks)

(iii) Find the highest common mode gain if the output is taken differentially. Assume that the tolerance of R_1 and R_2 are $\pm 2\%$.

(5 marks)

(iv) Find an expression for the common mode input impedance and calculate its value.

$\beta = 100 \qquad V_A = 85V \qquad r_\mu = \infty$

(5 marks)

QUESTION TWO *(25 marks)*

An enhancement mode NMOS amplifier shown in Figure-Q2. Assume that the devices Q_1 and Q_2 are matched.

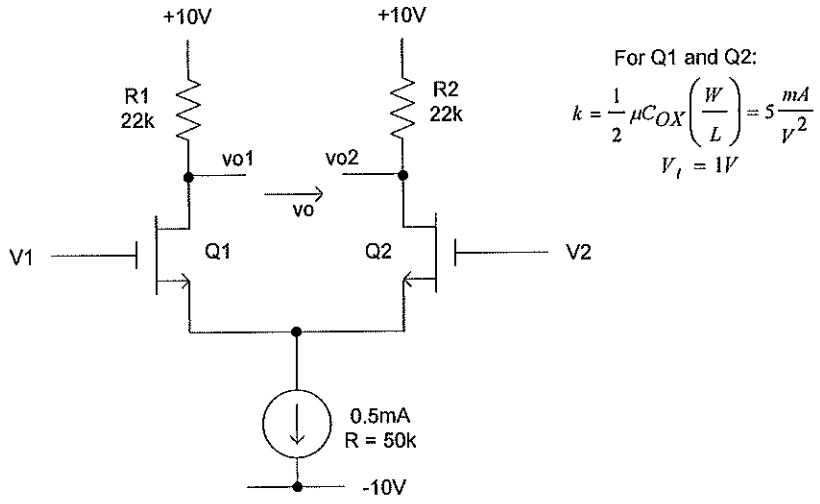

Figure - Q2

(a) When no input signal is present, find the differential input voltage $V_D = V_1 - V_2$ required if $V_{D1} = 10V$.

(6 marks)

(b) Draw the differential half circuits for the ac signals and derive expressions for the voltage gains $\frac{v_{o1}}{v_d}, \frac{v_{o2}}{v_d}, \frac{v_o}{v_d}$ and calculate their values. The differential input signal voltage $v_d = v_1 - v_2$ and symmetric dc biasing is used at the gates.

(9 marks)

(c) Find the value of common mode gain for single ended output and calculate the $CMRR$ in dB.

(6 marks)

(d) Estimate the input offset voltage using following data.

Tolerance of resistors $R_1, R_2 = \pm 3\%$

Tolerance of $\left(\frac{W}{L}\right)$ ratio $= \pm 5\%$

You may assume that the tolerance of other parameters are negligible.

(4 marks)

QUESTION THREE *(25 marks)*

(a) An integrated circuit amplifier is shown in Figure-Q3(a). Assume that the transistors are matched and $\beta = 100$ and $V_A = 80V$.

(i) What is the function of Q_1 and Q_3? Calculate the collector current of Q_1 at no signal.
(3 marks)

(ii) Derive an expression for the voltage gain $\frac{v_o}{v_{in}}$ and calculate its value.
(6 marks)

(iii) If this amplifier is connected to a load of $75k$, find the resulting voltage gain.
(4 marks)

(iv) Derive the input impedance R_{in} and the output impedance R_o.
(4 marks)

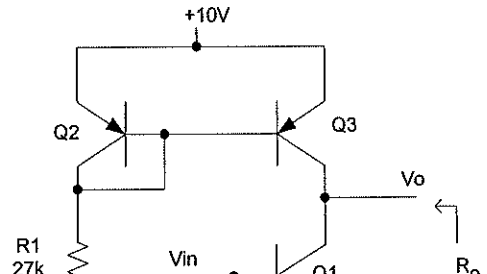

Figure-Q3(a)

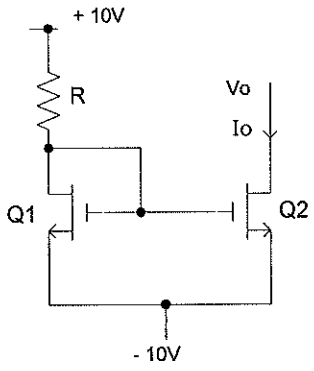

Figure-Q3(b)

(b) A current mirror implemented with NMOS devices is shown in Figure-Q3(b). You may use the data given below.

$L_1 = L_2 = 5\mu m$ $W_2 = 50\mu m$ $|V_t| = 2V$ $\mu C_{OX} = 65\frac{\mu A}{V^2}$

$V_A = 80V$ $I_o = 250\mu A$ $I_{ref} = 50\mu A$

(i) Calculate the value of W_1 proving any formula you use.
(5 marks)

(ii) Find the value of the resistance R.
(3 marks)

QUESTION FOUR (*25 marks*)

(a) Derive the necessary and sufficient condition that must be satisfied by a sinusoidal oscillator to function.

(5 marks)

(b) Consider the oscillator circuit shown in Figure-Q4.

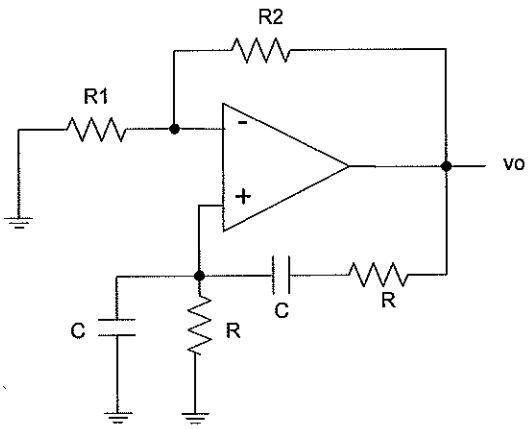

Figure -Q4

(i) Derive an expression for loop gain and hence find the frequency of oscillation. How do you determine R_1 and R_2?

(10 marks)

(ii) Calculate component values for a oscillation frequency of 50KHz satisfying the bounds, that any resistor value $> 2k$ and any capacitor value $> 0.5nF$.

(5 marks)

(iii) Suggest a modification to this circuit to ensure sinusoidal output. You may not need to find any component values.

(5 marks)

QUESTION FIVE (25 *marks*)

Consider the Class B amplifier shown in Figure-Q5.

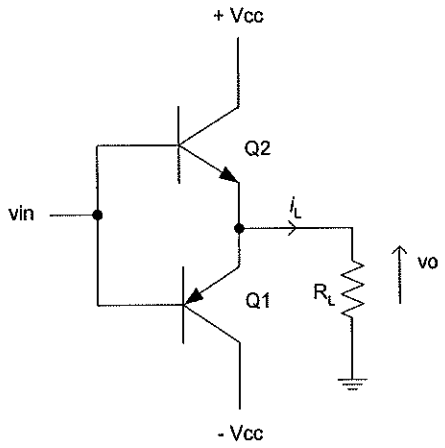

Figure - Q5

(a) Derive an expression for power efficiency of the circuit and calculate the maximum efficiency possible.

(7 marks)

(b) Find an expression for the maximum power dissipated by each device and power delivered to the load at that instance.

(7 marks)

(c) The amplifier uses a supply of $\pm 20V$ and delivers $15W$ to an 8Ω load. Find the peak current drawn from the supply, the total supply power, power conversion efficiency and the maximum power dissipation of each transistor.

(11 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.