UNIVERSITY OF ESWATINI

MAIN EXAMINATION, FIRST SEMESTER

DECEMBER 2019

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER:	ANALOGUE ELECTRONICS II
COURSE CODE:	EEE421
TIME ALLOWED:	THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question you may assume any reasonable values.
3. Some useful formulas are given in the last page.

THIS PAPER SHOULD NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR

THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

A circuit of a differential amplifier is shown in Figure-Q1.

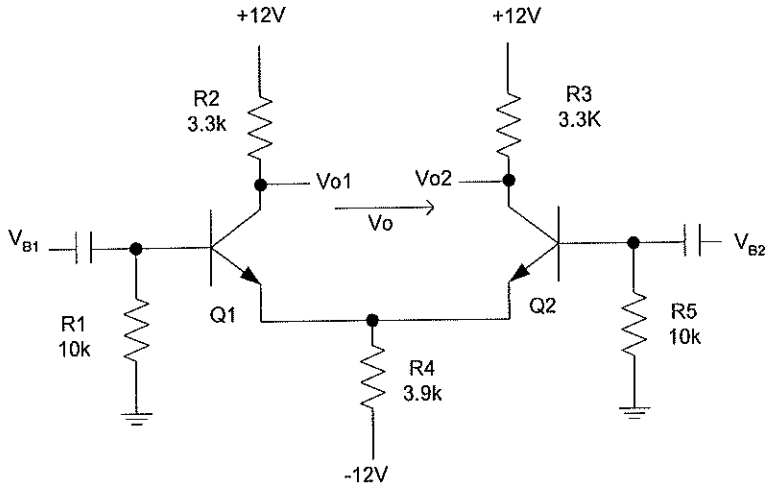

Figure - Q1

(a) If the transistors are of high gain type and matched, find the collector currents of the two transistors at no signal. What the voltages at the collectors and at the emitters?

(6 marks)

(b) (i) When a differential input signal v_d is applied to the circuit, derive the expressions drawing differential half circuits for the voltage gains $\frac{v_{01}}{v_d}$, $\frac{v_{02}}{v_d}$ and $\frac{v_o}{v_d}$.

(6 marks)

(ii) Calculate the values of the gains in (i) above.

(4 marks)

(c) (i) Find an expression for the differential input impedance and calculate its value if $\beta = 150$.

(3 marks)

(ii) Estimate the input offset voltage, input bias current and the input offset current of the amplifier using the following data.

Tolerance of resistors $= \pm 5\%$

Tolerance of scale currents $= \pm 20\%$

Tolerance of β $= \pm 20\%$

Value of β $= 150$

Assume that the tolerances of R_1, R_5 and R_4 are negligible.

(6 marks)

QUESTION TWO *(25 marks)*

Consider the NMOS amplifier shown in Figure-Q2. Assume that the devices Q_1 and Q_2 are matched.

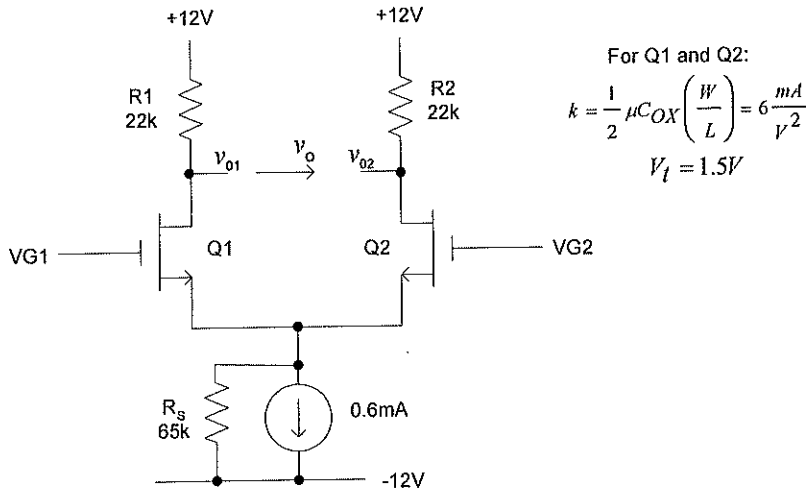

Figure - Q2

(a) If $V_{G1} = V_{G2} = 2V$, find the dc voltages at the drain and the source of the transistors.

(6 marks)

(b) If V_{G1} and V_{G2} are changed independently until $I_{D1} = 0.6mA$, calculate the value of differential input voltage applied.

(5 marks)

(c) When a common mode signal v_{cm} is applied to both inputs, find the common mode gain $\frac{v_{o1}}{v_{cm}}$ and $CMRR$. Prove any formula of the gain you use.

(6 marks)

(d) If R_1 and R_2 are having tolerances of $\pm 5\%$, find the common mode gain $\frac{v_o}{v_{cm}}$ and $CMRR$.

(8 marks)

QUESTION THREE *(25 marks)*

(a) A current source implemented with BJTs is shown in Figure-Q3(a). The transistors are of high gain type and matched.

(i) Derive an expression for the reference current to show how it is related to Io .

(4 marks)

(ii) Show the implementation of this current source for $I_o = 125\mu A$ deriving the component values. Assume that the $V_{BE} = 0.65V$ when the collector current is $0.8mA$, for the transistors you are going to use.

(6 marks)

(iii) Calculate the output resistance R_o if $V_A = 120V$ and the $\beta = 100$.

(3 marks)

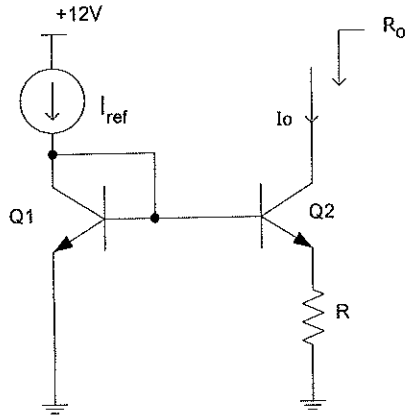

Figure-Q3 (a)

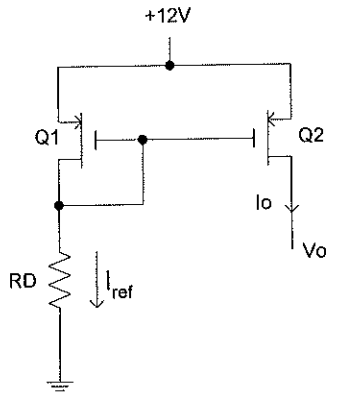

Figure-Q3 (b)

(b) A current mirror using PMOS devices is shown in Figure-Q3(b). Some of the device and circuit parameters are as follows.

$L_1 = L_2 = 6\mu m$ $W_2 = 60\mu m$ $|V_t| = 2V$ $\mu C_{OX} = 35\frac{\mu A}{V^2}$

$V_A = 75V$ $I_o = 125\mu A$ $I_{ref} = 70\mu A$

(i) Calculate the value of W_1 proving any formula you use.

(4 marks)

(ii) Find the resistance of R_D.

(3 marks)

(iii) When $V_o = 7V$, find the actual value of the output current I_o.

(5 marks)

QUESTION FOUR (*25 marks*)

A cascode amplifier is shown in Figure-Q4.

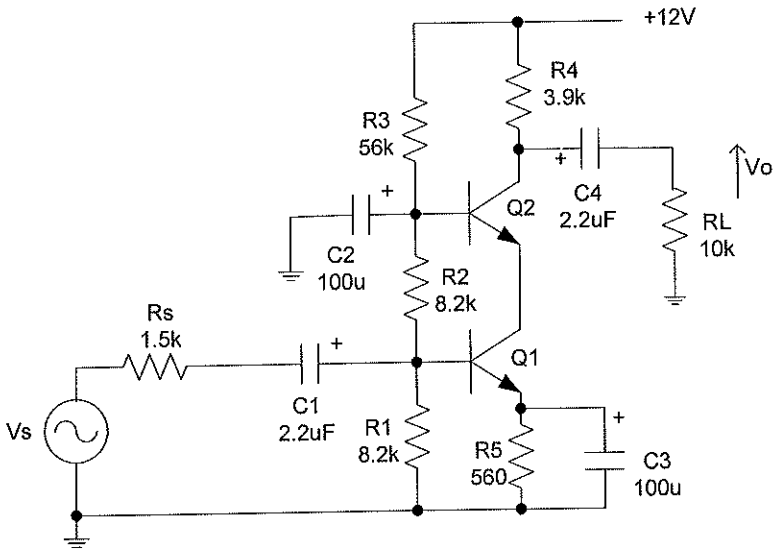

Figure-Q4

(a) Find the collector currents and collector voltages of each transistor assuming that the devices are identical and of high gain type.

(6 marks)

(b) Following parameters are given for the transistors, assuming usual notation.

$\beta = 100$ $C_\pi = 15pF$ $C_\mu = 5pF$ $r_o \gg$

(i) Derive an expression for the mid-band gain $\frac{v_o}{v_s}$ and calculate its value.

(8 marks)

(ii) Calculate the upper cut off frequency f_H using the Miller's components.

(8 marks)

(iii) What is the unity gain crossover frequency f_T of the amplifier.

(3 marks)

QUESTION FIVE (25 *marks*)

(a) Consider the circuit shown in Figure-5(a).

(i) Derive expressions for the frequency of oscillation, R_1 and R_2.

(8 marks)

(ii) Calculate all component values of the circuit for an oscillation frequency of $20kHz$. You may use capacitor values $> 0.5nF$.

(4 marks)

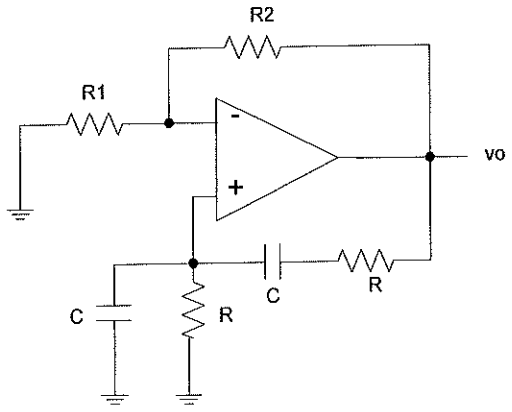

Figure -Q5(a)

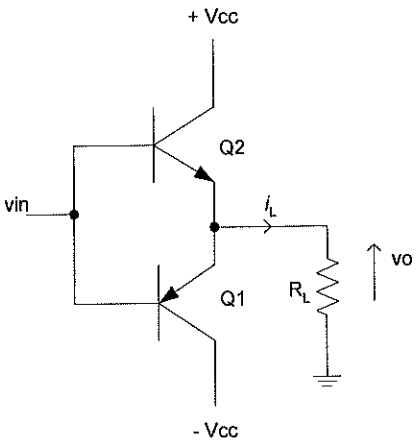

Figure - Q5(b)

(b) A power amplifier is shown in Figure-Q5(b).

(i) Derive expressions for power efficiency and power dissipated by each device.

(6 marks)

(ii) If the amplifier delivers $18W$ in to a 8Ω load, find the efficiency and power dissipation in transistors. What is the worst case power dissipation expected in a transistor? Assume $V_{cc} = 20V$.

(7 marks)

1. SOME USEFUL MOSFET EQUATIONS

$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$ in triode region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2$ in saturation region

$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - v_t)^2(1 + \lambda v_{DS})$ in saturation region with Channel Modulation effect

$V_A = \frac{1}{\lambda}$

2. Unless otherwise stated $V_{BE(ON)} = 0.6V$ and $V_T = 0.025V$.