UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF PHYSICS

2006/2007
MAIN EXAMINATION

Title of the Paper: **DIGITAL ELECTRONICS**
Course Number: **P411**
Time Allowed: **Three Hours.**

Instructions:
1. To answer, pick any five out of seven questions in the following pages.
2. Each question carries 20 points.
3. This paper has 8 pages, including this page.

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QUESTION 1:

a: Transform the Truth Table below into (10 marks)

(i). a K-Map,

(ii). a function in the following format (a SOP):

$F_1(B, C, D, E) = \Sigma(n1, n2, - - -, nB, nC, - - -, nF)_{hex}$

(iii). a function in the following format (a POS):

$F_2(B, C, D, E) = \prod(n1, n2, - - -, nB, nC, - - -, nF)_{hex}$

The number in the above brackets must be hexadecimal.

b: Prove $F_1 = F_2$. (must have equations to support) (10 marks)

BCDE	F	BCDE	F
0000	0	1000	0
0001	1	1001	1
0010	1	1010	0
0011	0	1011	0
0100	0	1100	0
0101	1	1101	1
0110	0	1110	1
0111	0	1111	1

QUESTION 2:

Using the tabulation method, simplify the following Boolean function F into the SOP answer:

$F(v, w, x, y, z) = \Sigma(0, 4, 9, B, C, D, E, F, 10, 11, 12, 13, 14, 16, 1E)_{hex}$

(hex number in the brackets of the above function) (20 marks)

QUESTION 3:

a: With the help of a K-map, obtain the simplified expressions in (i) SOP and (ii) POS of the following Boolean Function. In the equations, "d" represents the don't-care conditions.

$$F(W,X,Y,Z) = \overline{X}Y(\overline{W}+\overline{Z}) + \overline{X}(\overline{WY}+W\overline{Z}) + \overline{W}XYZ\,,$$
$$d(W,X,Y,Z) = \overline{W}X(\overline{Y}Z+Y\overline{Z}) + WYZ$$

(10 marks)

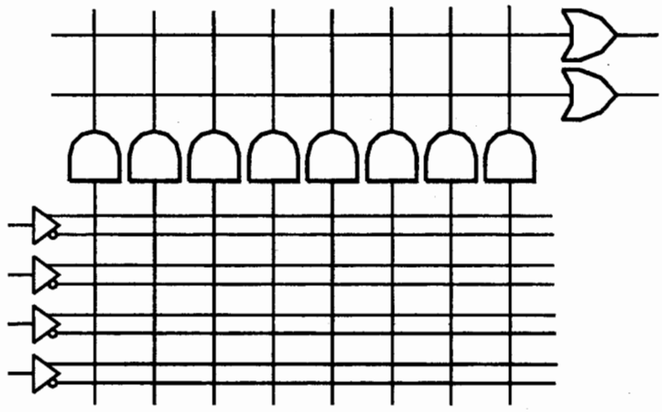
b: Implement the Boolean function, $F(A,B,C,D,E) = \overline{A}C\overline{E} + \overline{C}D(AB + \overline{AB})$, with only NAND gates and nothing but NAND gates. Complement inputs are available only at input terminals, nowhere else. The implement must have its support function.

(10marks)

QUESTION 4:

a: Implement the following function with a multiplexer (must have this component) of 2-bit select address vw and other elementary gates:
$F(v, w, x, y) = \Sigma(0, 1, 5, 7, 9, A, F)_{hex}$
(hex number in the brackets of the above function) (10 marks)

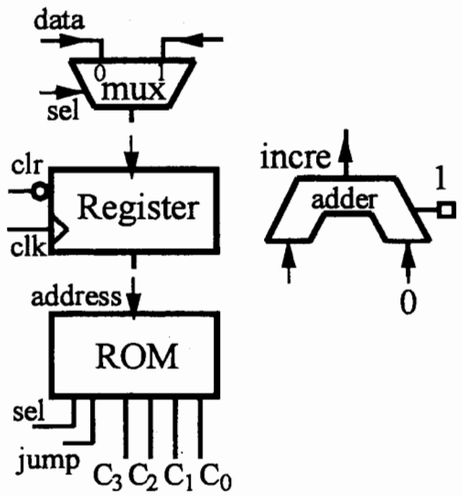
b: Implement the function given in (a) with a PAL structure. Simplification is required. (10 marks)



QUESTION 5:

a: In the figure below is a micro-programmed sequencer (the circuit is not complete yet). In the ROM, there are fields in a byte: jumping address, mux select address, and sequence output, C. First, complete the circuit wiring to make the sequencer have a proper function as listed in the ROM table. Next, find the sequence output, C, that the processor runs through. The sequencer starts at address 0000 and finally jumps back to 0000.

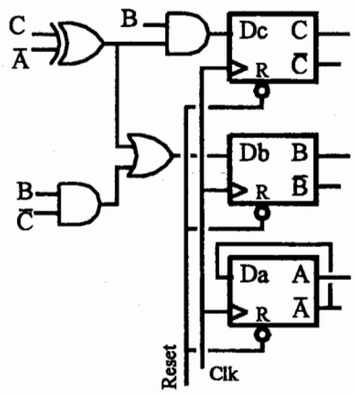
(10 marks)



ROM addr	ROM contents		
	sel	jump	C
0	1	x	A
1	1	x	2
2	1	x	4
3	0	B	7
4	1	x	C
5	1	x	F
6	1	x	9
7	0	0	4
8	1	x	1
9	1	x	3
A	0	E	E
B	1	x	5
C	1	x	D
D	1	x	0
E	0	6	0
F	0	0	6

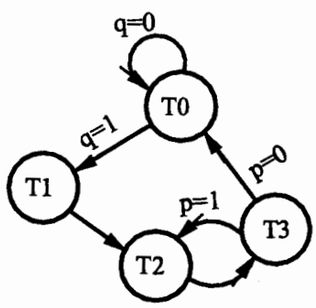
b: Below is a synchronous sequencer of 3-D/ff. Starting from ABC=000, what sequence does the circuit step through? Is there any external control to change the sequence?

(10 marks)



QUESTION 6:

Consider below the state diagram with two external control signals p and q. The states in the diagram are assigned as T0 to T2. On the paths where there is no control, are don't care case. Design, with D-ff's, a clocked sequencer to cycle repeatedly through the states determined by the state diagram. First obtain from the state diagram, for all control combinations from 00 to 11, all the possible sequences starting from T0. Then, obtain a state table, ff input functions, and a logic circuit. (hint: 2-bit memory is enough) (20 marks)



QUESTION 7:

Assume that two n-bit binary integer numbers, B_{n-1}---B_1B_0 and A_{n-1}---A_1A_0 are to be compared. The comparator has three outputs: "B=A", "B>A", and "B<A". Design and draw an ASM chart only to implement the function of this comparator. Assume before starting: "n" is already stored in the counter (Cntrn), "B" number in the register (Regb), and "A" number in (Rega).
(hint: shl ⇒ register operation shifted one bit to the left; shr ⇒ register operation shifted one bit to the right; decr1 ⇒ counter operation decreased by 1)

(20 marks)