UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, FIRST SEMESTER 2007/8

FACULTY OF SCIENCE

DEPARTMENT OF PHYSICS

TITLE OF PAPER: DIGITAL ELECTRONICS

COURSE CODE: P411

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. **There are six questions in this paper. Answer any FIVE questions.**
2. **Each question carries 20 marks.**

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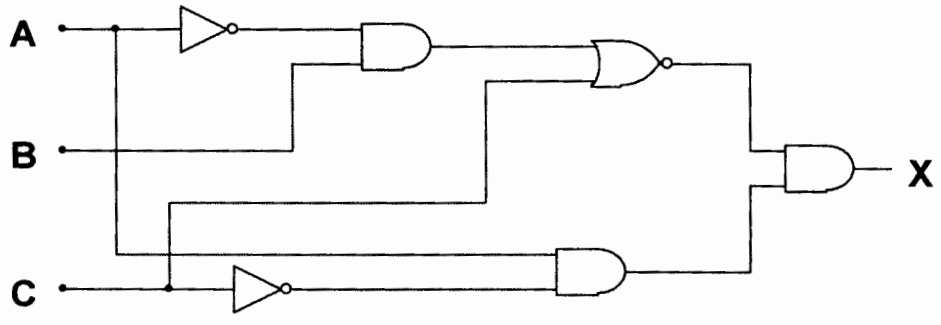
THIS PAPER CONTAINS SEVEN (7) PAGES INCLUDING THIS PAGE

QUESTION ONE ***(20 marks)***

(a) Implement the Boolean expression $W = X\overline{Y} + \overline{X}Y$ using only NOR gates.

(7 marks)

(b) Obtain the Boolean expression for the following combinational logic circuit, simplify the expression and implement it using a minimal number of AND, OR and NOT gates. *(7 marks)*



(c) Explain why NOR gates are considered as universal gates.

(6 marks)

QUESTION TWO ***(20 marks)***

An engine monitoring system has 4 inbuilt sensors which together output a 4-bit binary number. You are to design a logic circuit which takes the 4-bit binary number and outputs a RED light warning light when the decimal equivalent of the binary number is 0 to 3 and 12 to 15, a GREEN light when the value is 8 to 10 and an AMBER light when the binary value is 3 to 7 and 11 to 13.

(a) Draw up the truth table. *(4 marks)*

(b) Implement the truth table using a minimal number of AND, OR and NOT gates. *(10 marks)*

(c) Implement the table using 16 to 1 multiplexers. *(4 marks)*

(d) Comment on the two methods of implementation. *(2 marks)*

QUESTION TRHEE ***(20 marks)***

(a) Explain how a 4-input multiplexer can be used as a universal 2-input logic gate. Are there any new gates not ordinarily implementable with one standard gate element? If so which ones are they? *(7 marks)*

(b) Minimize the following Boolean expression and show how a hazard-free implementation may be obtained.

$F = \overline{(AB)} \oplus (\overline{A}C) + \overline{C} \oplus BD$ *(7marks)*

(c) Design a circuit using a ROM which takes a 3-bit binary number and outputs a binary value equal to the sum of this number and its square i.e. number + number^2.

(6 marks)

QUESTION FOUR ***(20 marks)***

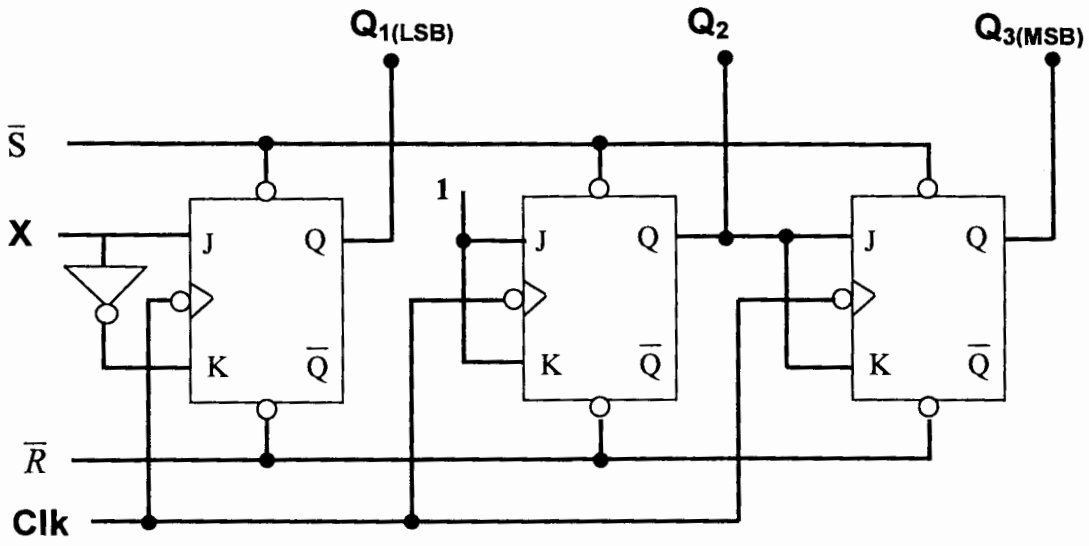
(a) Describe the operation of the 3 flip-flops in the sequential circuit below. The input **X** can be either 0 or 1. *(5 marks)*

(b) Draw the transition tables and the state diagrams for X = 0 and for X = 1.

(12 marks)

(c) Comment on the counting sequences in the two cases X = 0 and X = 1.

(3 marks)



QUESTION FIVE ***(20 marks)***

(a) Draw a logic gate level diagram of a clocked, level triggered D-Type flip-flop.

(2 marks)

(b) Show how D-Type flip-flops and any other circuit components can be used to realize:

(i) A 4-bit serial-to-parallel converter. *(2 marks)*

(ii) A 4-bit parallel-to-serial converter. *(6 marks)*

(c) A synchronous 3-bit binary counter progresses through the sequence:

000, 010, 100, 110, 001, 011, 101, 111, and repeats.

Design and implement this counter with a minimal number of D-Type flip-flops and logic gates.

(10 marks)

QUESTION SIX ***(20 marks)***

(a) Briefly describe the functional differences between RAMs, ROMs and Flash Memories. *(6 marks)*

(b) Show how a **128k x 8 RAM** can be built using **64k x 4 RAM** chips. *(6 marks)*

(c) How would you electronically add two 4-bit numbers? Illustrate your answer with an appropriate logic diagram. *(5 marks)*

(d) Explain what you understand by each of the following: parity generator, ring counter, decoder. *(3 marks)*