UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF PHYSICS

MAIN EXAMINATION	2008/2009
TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER :	P411
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ALL QUESTIONS.

EACH QUESTION CARRIES 20 MARKS.

MARKS FOR DIFFERENT SECTION ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS 5 PAGES INCLUDING THIS PAGE.

DO NOT OPEN THE PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

1 (a) State De Morgan's theorems. [4]

(b) Simplify the following expressions using Boolean algebra:

(i) $F = \left(X + \overline{Y} + \overline{X} \cdot Y\right) \cdot \overline{Z}$ [2]

(ii) $F = \overline{X} \cdot Y \cdot \left(X + \overline{Y} + \overline{X} \cdot Y\right)\left(X + \overline{Y}\right)$ [2]

(c) Given that:

$$F = W \cdot X \cdot \overline{Y} \cdot Z + W \cdot \overline{X} \cdot \overline{Y} \cdot \overline{Z} + \overline{X} \cdot Y + \overline{W} \cdot \overline{X} + \overline{W} \cdot X \cdot \overline{Y} \cdot Z$$

(i) Use a Karnaugh Map to simplify F. [7]

(ii) Draw the logic circuit using only NAND gates for the simplified F expression. [2]

(iii) Identify any static hazards and show how the hazards can be eliminated using a K-Map. [1]

(iv) Following from (iii), draw the logic circuit but using only 2-input NAND gates. [2]

2 (a) Toyee-Toyee Private Limited, a local company engaged in reverse engineering of electronic toys has sent you 4 logic circuit diagrams in **Appendix A**. Name each circuit (e.g. D-type Flip-Flop), label the inputs and outputs (e.g. A,B,C data input), and determine the truth table. **[5 each]**

3 (a) In the context of digital electronics, explain the terms:

(i) Register [2]

(ii) Counter [2]

(b) (i) Design a 4-bit upward counting ripple counter using negative edge-triggered JK flip-flops. [10]

(ii) Explain using at most 100 words how your design in 3b(i) operates. [4]

(iii) Explain in not more than 50 words what modifications to your design in **3b(i)** would produce a 4-bit downward ripple counter. [4]

4 (a) Write down the equation form for the binary to gray code conversion rule. [2]

(b) Convert the following into Gray-code.

(i) DE_{16} **[2]**

(ii) 714_8 **[2]**

(iii) 10000011_{BCD} **[3]**

(c) Confirm with a truth table if TRUE or FALSE that:

(i) NAND function is associative. **[3]**

(ii) XNOR function is not associative. **[3]**

(d) Design a 3 bit full adder using a 3-to-8 line decoder. **[5]**

5 (a) Write brief notes that also include truth tables, function tables, K-Maps, logic circuit diagrams, or Boolean expressions on any 2 of the following: **[10 each]**

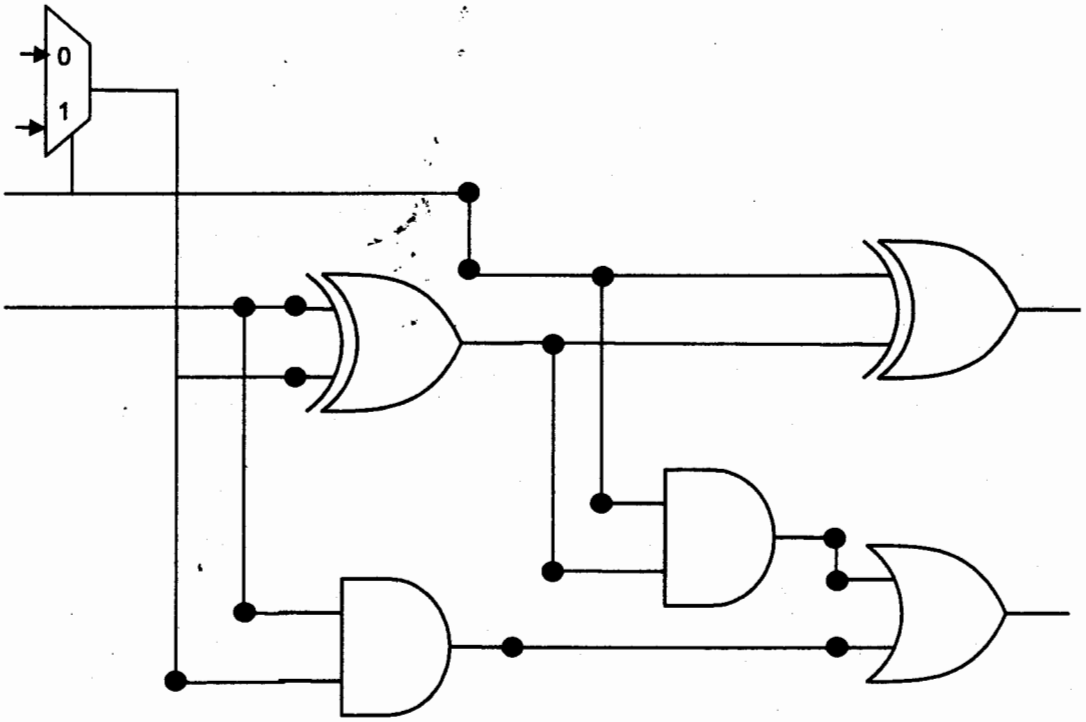
(i) Prime Implicant, Essential Prime Implicant, Distinguished 1-Cell.

(ii) Edge-triggered and clocked flip-flop.

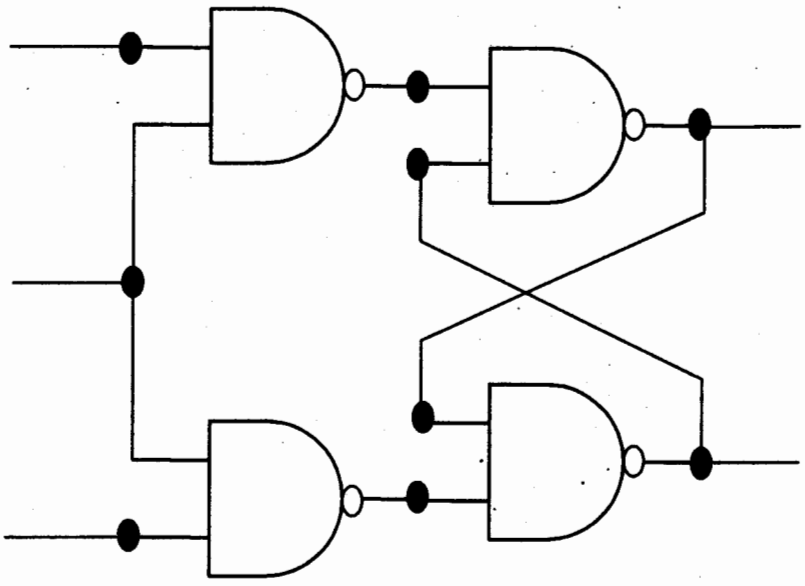
(iii) Combinational Logic and Sequential Logic Circuits

APPENDIX A – DATASHEET

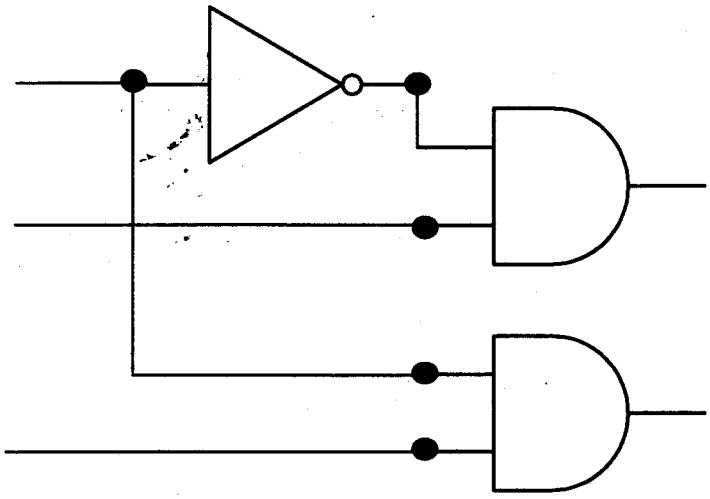
TOYEE-TOYEE PRIVATE LIMITED



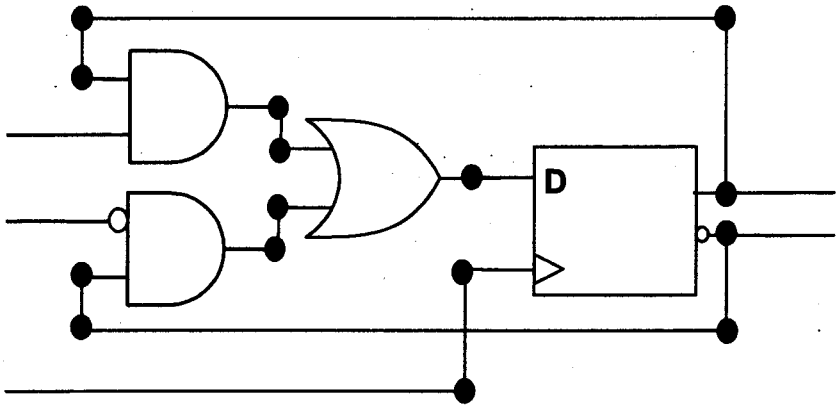
LOGIC CIRCUIT 1



LOGIC CIRCUIT 2



LOGIC CIRCUIT 3



LOGIC CIRCUIT 4