UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF PHYSICS

MAIN EXAMINATION	2009/2010
TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER:	P411
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ANY FOUR OUT OF SIX QUESTIONS.

EACH QUESTION CARRIES 25 MARKS.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS 9 PAGES INCLUDING THIS PAGE.

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1 (a) (i) Convert 25.625_{10} to its binary equivalent. **[3]**

(ii) Convert the number 101.101_2 to its decimal equivalent. **[3]**

(b) (i) Find the equivalent decimal value for the BCD coded number: 0001010001110101. **[3]**

(ii) Convert the hexadecimal number F8E6 to the corresponding decimal number. **[3]**

(c) (i) Add $(AECF1)_{16}$ and $(15ACD)_{16}$. **[3]**

(ii) Subtract $(3A7)_{16}$ from $(1274)_{16}$. **[3]**

(d) (i) Give two drawbacks of dealing with negative numbers in digital computers using the signed magnitude method. **[3]**

(ii) Using the 2's complement, subtract 1010_2 from 1101_2 and check your result using the decimal equivalents of these numbers. **[4]**

2 (a) Derive the truth tables for the action of the circuits in **figures 1** and **2** of the **Appendix A** and hence state the logic functions that they perform. **[6]**

(b) Explain the action of the circuit in **figure 3** of the **Appendix A** and derive its truth table. What kind of gate is it? **[4]**

(c) Use only AND, OR and NOT gates to construct a logic circuit that carries out the following logic function:

$$F = \overline{(A\bar{C} + \bar{B})} + BC.$$ **[4]**

(d) Convert the following logical expression into canonical Product of Sums (maxterms) form:

$$F = (A + B)(A + C)(B + C).$$ **[7]**

(e) Use a Karnaugh map to simplify the following logic expression:

$$F = \bar{A}\bar{B}\bar{C} + \bar{A}B + AB\bar{C} + AC.$$ **[4]**

3 (a) What logic function is performed by the interconnected NAND gates in **figure 4** of the **Appendix A**. You are not required to simplify the function. **[3]**

(b) Define the following terms:

(i) Fan in and fan out; **[2]**

(ii) Current hogging in DCTL logic; **[2]**

(iii) Race hazard, with an example. **[2]**

(c) Draw a well labeled logic circuit of a two-NAND gate RS flip flop (or a bistable multivibrator) and explain the way it functions as a memory element. **[6]**

(d) **Figure 5** in the **Appendix A** is a logic diagram of a clocked four-NAND gate *SR* flip flop. Study it and answer the questions that follow:

(i) Why is the flip flop clocked? **[2]**

(ii) Explain how the *S* and *R* inputs are transmitted through the first and second pairs of NAND gates to give the Q AND $\bar{Q}$ outputs. **[4]**

(iii) What is the memory capacity of this flip flop? **[2]**

(iv) What is the major disadvantage of this flip flop? **[2]**

4 (a) Explain what is meant by 'level triggering', 'negative-edge triggering' and 'leading edge triggering' of a flip flop. **[3]**

(b) **Figure 6** in the **Appendix A** is a logic diagram of a clocked *D*-type flip flop. Answer the following questions with reference to that figure:

(i) What is the advantage of having a single input to the latch? **[1]**

(ii) What is the function of the gate labeled *N5*? **[1]**

(iii) Complete the following table for the various signals applied to the inputs. **[4]**

Input			Outputs before the clock pulse		Outputs after the clock pulse	
D	S	R	Q	$\bar{Q}$	Q	$\bar{Q}$
0	0	1	1	0		
0	0	1	0	1		
1	1	0	1	0		
1	1	0	0	1		

(c) **Figure 7** in the **Appendix A** is a logic diagram of a *JK* flip flop. State the behavior of the flip flop when the *J* and *K* inputs assume the following values at the triggering of the clock:

(i) $J = K = 1$; **[2]**

(ii) $J = 1$ and $K = 0$; **[2]**

(iii) $J = 0$ and $K = 1$; **[2]**

(iv) $J = 0$ and $K = 0$. **[2]**

(d) (i) Explain how the modulus of a counter is determined, using an example. **[2]**

(ii) **Figure 8** in the **Appendix A** represents a mod-8 counter. Verify the counter's performance by way of a timed waveform diagram of the outputs Q0, Q1 and Q2. Show, clearly, the triggering points and counting sequence on your diagram. **[6]**

5 (a) Minimize the Boolean expression for the four variable logic function

$F(A,B,C,D) = \sum m(0,2,6,8,9)$

using a Karnaugh map. **[6]**

(b) Make the truth table for a full adder and develop its logic circuit using a 3 to 8 decoder. **[6]**

(c) Make a truth table for a 4 to 3 priority encoder. State the order of priority of the inputs. **[6]**

(d) Design a 2 to 1 multiplexer (2:1 mux) by first minimizing its Boolean operational function using a Karnaugh map of its truth table. **[7]**

6 (a) Distinguish between a microprocessor and a microcontroller, giving an example of each. **[4]**

(b) Briefly explain the functions of the following parts of a microprocessor unit:

(i) Accumulator (ACC); **[2]**

(ii) Data register (DR); **[2]**

(iii) Flag register (FR); **[2]**

(iv) Address register (AR); **[2]**

(v) Arithmetic logic unit (ALU); **[2]**

(vi) Program counter (PC); **[1]**

(vii) Instruction decoder. **[1]**

(c) Explain the following modes of addressing in assembly language:

(i) Inherent or implied addressing; **[2]**

(ii) Immediate addressing; **[2]**

(iii) Indirect addressing. **[2]**

(d) Using **Appendix B** to convert your mnemonics into opcodes in Hex, write an assembly language program to perform the following operations:

(i) Load 93H into the accumulator A; **[0.5]**

(ii) Load B7H into register C; **[0.5]**

(iii) Add both contents; **[0.5]**

(iv) Add the number 35H directly to the sum; **[0.5]**

(v) Save the sum in register D; **[0.5]**

(vi) End the program. **[0.5]**

APPENDIX A – DIAGRAMS

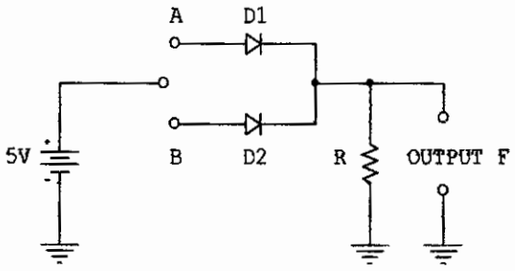

Figure 1

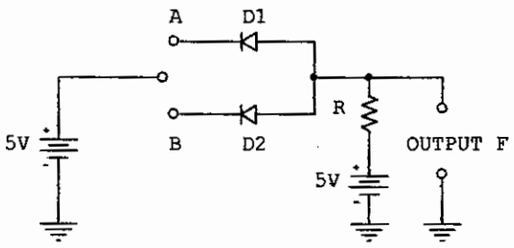

Figure 2

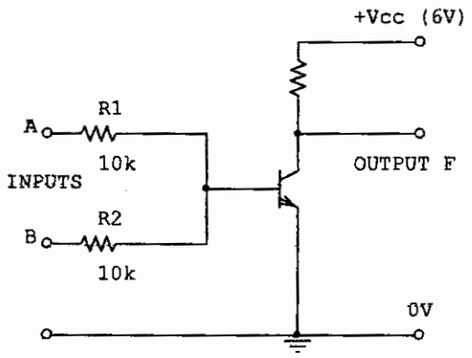

Figure 3

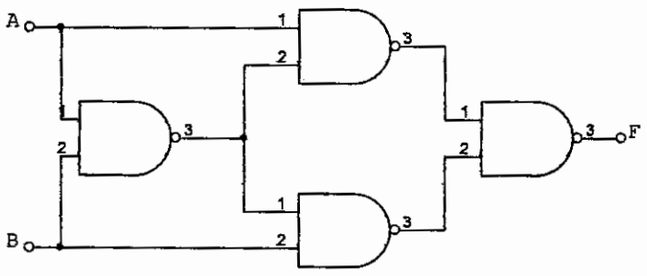

Figure 4

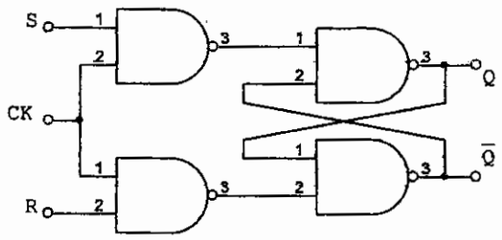

Figure 5

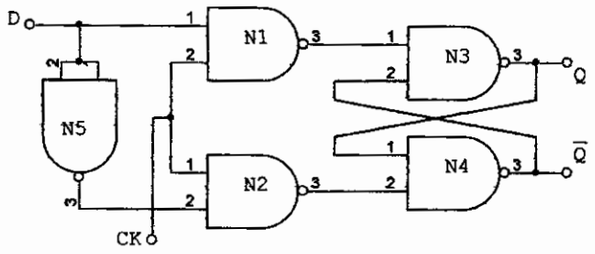

Figure 6

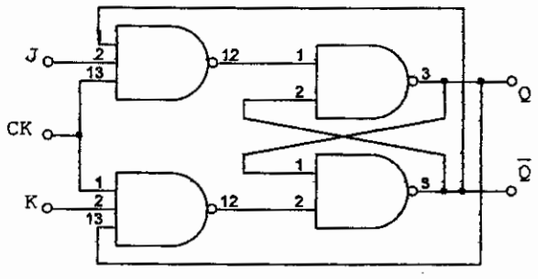

Figure 7

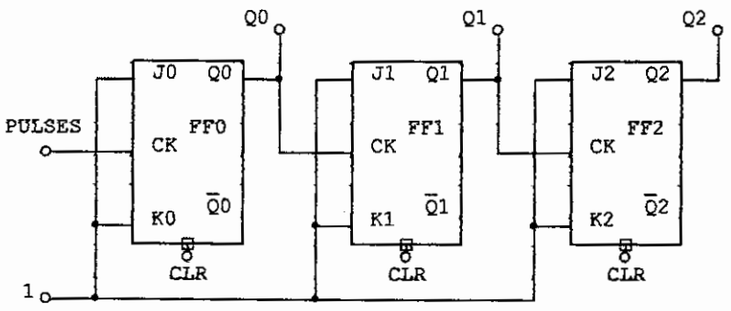

Figure 8

APPENDIX B – 8085 MNEMONICS

JUMP	CALL	RETURN	MOVE	
C3 JMP	CD CALL	C9 RET	40 MOV B,B	60 MOV H,B
C2 JNZ	C4 CNZ	C0 RNZ	41 MOV B,C	61 MOV H,C
CA JZ	CC CZ	C8 RZ	42 MOV B,D	62 MOV H,D
D2 JNC	D4 CNC	D0 RNC	43 MOV B,E	63 MOV H,E
DA JC	DC CC	D8 RC	44 MOV B,H	64 MOV H,H
E2 JPO	E4 CPO	E0 RPO	45 MOV B,L	65 MOV H,L
EA JPE	EC CPE	E8 RPE	46 MOV B,M	66 MOV H,M
F2 JP	F4 CP	F0 RP	47 MOV B,A	67 MOV H,H
FA JM	FC CM	F8 RM		
E9 PCHL			48 MOV C,B	68 MOV L,B
			49 MOV C,C	69 MOV L,C
MOVE	Acc	LOAD	4A MOV C,D	6A MOV L,D
IMMEDIATE	IMMEDIATE	IMMEDIATE	4B MOV C,E	6B MOV L,E
			4C MOV C,H	6C MOV L,H
06 MVI B	C6 ADI	01 LXI B,	4D MOV C,L	6D MOV L,L
0E MVI C,	CE ACI	11 LXI D,	4E MOV C,M	6E MOV L,M
16 MVI D,	D6 SUI	21 LXI H,	4F MOV C,A	6F MOV L,A
1E MVI E,	DE SBI	31 LXI SP,		
26 MVI H,	E6 ANI			
2E MVI L,	EE XRI		50 MOV D,B	70 MOV M,B
36 MVI M,	F6 0RI	DOUBLE ADD	51 MOV D,C	71 MOV M,C
3E MVI A,	FE CPI		52 MOV D,D	72 MOV M,D
		09 DAD B	53 MOV D,E	73 MOV M,E
		19 DAD D	54 MOV D,H	74 MOV M,H
INCREMENT	DECREMENT	29 DAD H	55 MOV D,L	75 MOV M,L
		39 DAD SP	56 MOV D,M	
04 INR B	05 DCR B		57 MOV D,A	77 MOV M,A
0C INR C	0D DCR C			
14 INR D	15 DCR D	LOAD/STORE	58 MOV E,B	78 MOV A,B
1C INR E	1D DCR E		59 MOV E,C	79 MOV A,C
24 INR H	25 DCR H	0A LDAX B	5A MOV E,D	7A MOV A,D
2C INR L	2D DCR L	1A LDAX D	5B MOV E,E	7B MOV A,E
34 INR M	35 DCR M	2A LHLD	5C MOV E,H	7C MOV A,H
3C INR A	3D DCR A	3A LDA	5D MOV E,L	7D MOV A,L
			5E MOV E,M	7E MOV A,M
03 INX B	0B DCX B	02 STAX B	5F MOV E,A	7F MOV A,A
13 INX D	1B DCX D	12 STAX D		
23 INX H	2B DCX H	22 SHLD	ACCUMULATOR	
33 INX SP	3B DCX SP	32 STA		
			80 ADD B	A0 ANA B
			81 ADD C	A1 ANA C
RESTART	ROTATE	SPECIALS	82 ADD D	A2 ANA D
			83 ADD E	A3 ANA E
C7 RST 0	07 RLC	EB XCHG	84 ADD H	A4 ANA H
CF RST 1	0F RRC	27 DAA	85 ADD L	A5 ANA L
D7 RST 2	17 RAL	2F CMA	86 ADD M	A6 ANA M
DF RST 3	1F RAR	37 STC	87 ADD A	A7 ANA A
E7 RST 4		3F CMC		

EF RST 5
F7 RST 6
FF RST 7

CONTROL

00 NOP
20 RIM
30 SIM
76 HLT
F3 DI
FB EI

INPUT/OUTPUT

D3 OUT
DB IN

STACK OPS

C5 PUSH B
D5 PUSH D
E5 PUSH H
F3 PUSH PSW

C1 POP B
D1 POP D
E1 POP H
F1 POP PSW

E3 XTHL
F9 SPHL

88 ADC B
89 ADC C
8A ADC D
8B ADC E
8C ADC H
8D ADC L
8E ADC M
8F ADC A

90 SUB B
91 SUB C
92 SUB D
93 SUB E
94 SUB H
95 SUB L
96 SUB M
97 SUB A

98 SBB B
99 SBB C
9A SBB D
9B SBB E
9C SBB H
9D SBB L
9E SBB M
9F SBB A

A8 XRA B
A9 XRA C
AA XRA D
AB XRA E
AC XRA H
AD XRA L
AE XRA M
AF XRA A

B0 ORA B
B1 ORA C
B2 ORA D
B3 ORA E
B4 ORA H
B5 ORA L
B6 ORA M
B7 ORA A

B8 CMP B
B9 CMP C
BA CMP D
BB CMP E
BC CMP H
BD CMP L
BE CMP M
BF CMP A

END OF P411 EXAMINATION