UNIVERSITY OF SWAZILAND 155

FACULTY OF SCIENCE

DEPARTMENT OF PHYSICS

MAIN EXAMINATION	2010/2011
TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER:	P411
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ANY FOUR OUT OF SIX QUESTIONS.

EACH QUESTION CARRIES 25 MARKS.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS 6 PAGES INCLUDING THIS PAGE.

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1 (a) Find the equivalent Hex value for the BCD coded number 10101110101_{BCD}. **[7]**

(b) What is bus fight of logic gates and how can it be avoided? **[2]**

(c) Draw the circuit of a basic two-input TTL NAND gate with an open collector. **[2]**

(d) Explain what a wired-AND is, using an example. **[4]**

(e) Show that the output of three shorted open-collector NOR gates acts as a six input NOR gate. **[4]**

(f) What is the logic function, F, of the circuit in **Fig. 1** of the **Appendix A**? **[6]**

2 (a) Use any Karnaugh map as an example to distinguish between an implicant, a prime implicant and an essential prime implicant. **[6]**

(b) Use the Quine-McCluskey method to find the output function, F, in the truth table given in **Fig. 2** of the **Appendix B**; A,B,C and D are inputs. **[13]**

(c) Explain what a comparator does and how the two-input XNOR gate acts as a simple one-bit magnitude comparator. **[6]**

3 (a) Implement the function

$$f(x, y, z) = \sum m(1,2,6,7),$$

using a 4 to 1 multiplexer. **[6]**

(b) Implement the adder carry function $C(X, Y, Z)$ using a multiplexer. **[7]**

(c) Implement the adder sum function $S(X, Y, Z)$ using a multiplexer. **[8]**

(d) Design a Dual 4 to 1 Multiplexer-based full adder. **[4]**

4 (a) Explain what a parity bit is and make a truth table with three input bits, x, y and z producing one output odd parity bit P. **[5]**

(b) Show how you can implement P in (a) with a three-variable XNOR gate. **[5]**

(c) Make a truth table for a parity checker circuit which will have four inputs x, y, z and P with one output, E (error), which will be 1 whenever there is a parity error; E will be 1 whenever P is not the odd parity bit for the values of x, y and z. **[5]**

(d) Show that the function, E, in (c) can be implemented as an XNOR of the four input variables. **[7]**

(e) Make a figure in which a parity generator and parity checker are represented with block diagrams to show how data with a parity bit is transmitted and received. Include LEDs that indicate the values of P and E. **[3]**

5 (a) Design a 2 to 4 binary decoder with inputs S1, S0 and EN, where EN is an enable input. The outputs should be labeled Q0, Q1, Q2 and Q3. **[7]**

(b) Make a truth table for a 3 to 8 decoder and design one using 2 to 4 decoders. **[7]**

(c) Draw the logic circuit of a master-slave SR flip flop using NAND gates. **[5]**

(d) Construct a modulus 10 asynchronous decade counter and use it to explain what truncated states are. Use logic symbols for the flip flops without including their logic circuits. **[6]**

6 (a) Distinguish between volatile and non-volatile memory. **[2]**

(b) (i) What is the memory capacity of a cell with 8 bit locations from 000H to FFFH in Hex? **[5]**

(ii) How many address lines are required for the memory cell in (i)? **[3]**

(c) Most microprocessor units have a group of single bit registers called condition code registers or flags. Name three flags; you do not have to explain how they function. **[3]**

(d) (i) Explain, using an example, how repeated subtraction may be used to accomplish division. **[4]**

(ii) Draw a flowchart which shows the sequence of steps to be taken in accomplishing division by repeated subtraction on a microprocessor. Use **Appendix C** to write the corresponding assembly language mnemonics along side the flowchart for each step. You do not need to include the operation codes in Hex. **[8]**

APPENDIX A – DIAGRAM

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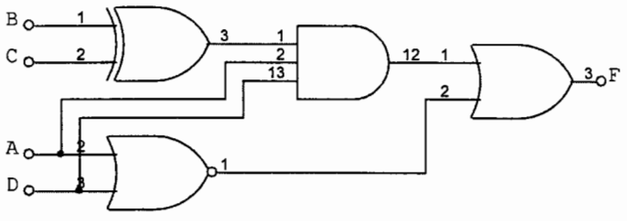

Figure 1

APPENDIX B – TRUTH TABLE

No.	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

Figure 2

APPENDIX C – 8085 MNEMONICS

JUMP	CALL	RETURN
C3 JMP	CD CALL	C9 RET
C2 JNZ	C4 CNZ	C0 RNZ
CA JZ	CC CZ	C8 RZ
D2 JNC	D4 CNC	D0 RNC
DA JC	DC CC	D8 RC
E2 JPO	E4 CPO	E0 RPO
EA JPE	EC CPE	E8 RPE
F2 JP	F4 CP	F0 RP
FA JM	FC CM	F8 RM
E9 PCHL		

MOVE IMMEDIATE	Acc IMMEDIATE	LOAD IMMEDIATE
06 MVI B	C6 ADI	01 LXI B,
0E MVI C,	CE ACI	11 LXI D,
16 MVI D,	D6 SUI	21 LXI H,
1E MVI E,	DE SBI	31 LXI SP,
26 MVI H,	E6 ANI	
2E MVI L,	EE XRI	
36 MVI M,	F6 0RI	DOUBLE ADD
3E MVI A,	FE CPI	
		09 DAD B
		19 DAD D
		29 DAD H
		39 DAD SP

INCREMENT	DECREMENT
04 INR B	05 DCR B
0C INR C	0D DCR C
14 INR D	15 DCR D
1C INR E	1D DCR E
24 INR H	25 DCR H
2C INR L	2D DCR L
34 INR M	35 DCR M
3C INR A	3D DCR A
03 INX B	0B DCX B
13 INX D	1B DCX D
23 INX H	2B DCX H
33 INX SP	3B DCX SP

RESTART	ROTATE	LOAD/STORE
C7 RST 0	07 RLC	0A LDAX B
CF RST 1	0F RRC	1A LDAX D
D7 RST 2	17 RAL	2A LHLD
DF RST 3	1F RAR	3A LDA
E7 RST 4		02 STAX B
		12 STAX D
		22 SHLD
		32 STA

SPECIALS
EB XCHG
27 DAA
2F CMA
37 STC
3F CMC

MOVE		
40 MOV B,B	60 MOV H,B	
41 MOV B,C	61 MOV H,C	
42 MOV B,D	62 MOV H,D	
43 MOV B,E	63 MOV H,E	
44 MOV B,H	64 MOV H,H	
45 MOV B,L	65 MOV H,L	
46 MOV B,M	66 MOV H,M	
47 MOV B,A	67 MOV H,H	
48 MOV C,B	68 MOV L,B	
49 MOV C,C	69 MOV L,C	
4A MOV C,D	6A MOV L,D	
4B MOV C,E	6B MOV L,E	
4C MOV C,H	6C MOV L,H	
4D MOV C,L	6D MOV L,L	
4E MOV C,M	6E MOV L,M	
4F MOV C,A	6F MOV L,A	
50 MOV D,B	70 MOV M,B	
51 MOV D,C	71 MOV M,C	
52 MOV D,D	72 MOV M,D	
53 MOV D,E	73 MOV M,E	
54 MOV D,H	74 MOV M,H	
55 MOV D,L	75 MOV M,L	
56 MOV D,M		
57 MOV D,A	77 MOV M,A	
58 MOV E,B	78 MOV A,B	
59 MOV E,C	79 MOV A,C	
5A MOV E,D	7A MOV A,D	
5B MOV E,E	7B MOV A,E	
5C MOV E,H	7C MOV A,H	
5D MOV E,L	7D MOV A,L	
5E MOV E,M	7E MOV A,M	
5F MOV E,A	7F MOV A,A	

ACCUMULATOR	
80 ADD B	A0 ANA B
81 ADD C	A1 ANA C
82 ADD D	A2 ANA D
83 ADD E	A3 ANA E
84 ADD H	A4 ANA H
85 ADD L	A5 ANA L
86 ADD M	A6 ANA M
87 ADD A	A7 ANA A

EF RST 5
F7 RST 6
FF RST 7

CONTROL

00 NOP
20 RIM
30 SIM
76 HLT
F3 DI
FB EI
2B BMI

INPUT/OUTPUT

D3 OUT
DB IN

STACK OPS

C5 PUSH B
D5 PUSH D
E5 PUSH H
F3 PUSH PSW

C1 POP B
D1 POP D
E1 POP H
F1 POP PSW

E3 XTHL
F9 SPHL

88 ADC B
89 ADC C
8A ADC D
8B ADC E
8C ADC H
8D ADC L
8E ADC M
8F ADC A

90 SUB B
91 SUB C
92 SUB D
93 SUB E
94 SUB H
95 SUB L
96 SUB M
97 SUB A

98 SBB B
99 SBB C
9A SBB D
9B SBB E
9C SBB H
9D SBB L
9E SBB M
9F SBB A

A8 XRA B
A9 XRA C
AA XRA D
AB XRA E
AC XRA H
AD XRA L
AE XRA M
AF XRA A

B0 ORA B
B1 ORA C
B2 ORA D
B3 ORA E
B4 ORA H
B5 ORA L
B6 ORA M
B7 ORA A

B8 CMP B
B9 CMP C
BA CMP D
BB CMP E
BC CMP H
BD CMP L
BE CMP M
BF CMP A

END OF P411 EXAMINATION