UNIVERSITY OF SWAZILAND

109

FACULTY OF SCIENCE

DEPARTMENT OF PHYSICS

MAIN EXAMINATION	:	2011
TITLE OF PAPER	:	ELECTRONICS I
COURSE NUMBER	:	P311
TIME ALLOWED	:	THREE HOURS
INSTRUCTIONS	:	ANSWER ANY FOUR OUT OF THE FIVE QUESTIONS
		EACH QUESTION CARRIES 25 MARKS
		MARKS FOR DIFFERENT SECTIONS ARE SHOWN IN THE RIGHT-HAND MARGIN

THIS PAPER HAS 6 PAGES, INCLUDING THIS PAGE.

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QUESTION 1

(a) Draw a small signal model of a bipolar junction transistor and label it. (2 marks)

(b) Use the model to derive the exact (not approximate) expression for the current gain of the transistor. (3 marks)

(c) Fig. 1 shows a fully-stabilised voltage amplifier. Explain, in detail, how the amplifier works, with reference to the functions of the resistors and capacitors used to build it. Justify the use of the term 'fully-stabilised'. What are the advantages of this amplifier in comparison with the fixed bias type shown in Fig. 2? (10 marks)

(d) The silicon transistor of Fig. 2 is biased for constant base current. If $\beta = 80$, $V_{CEQ} = 8$ V, $R_C = 3\text{k}\Omega$, and $V_{CC} = 15$ V, find

(i)	I_{CQ}.	(2 marks)
(ii)	R_B.	(5 marks)
(iii)	R_B if the transistor were a germanium device.	(3 marks)

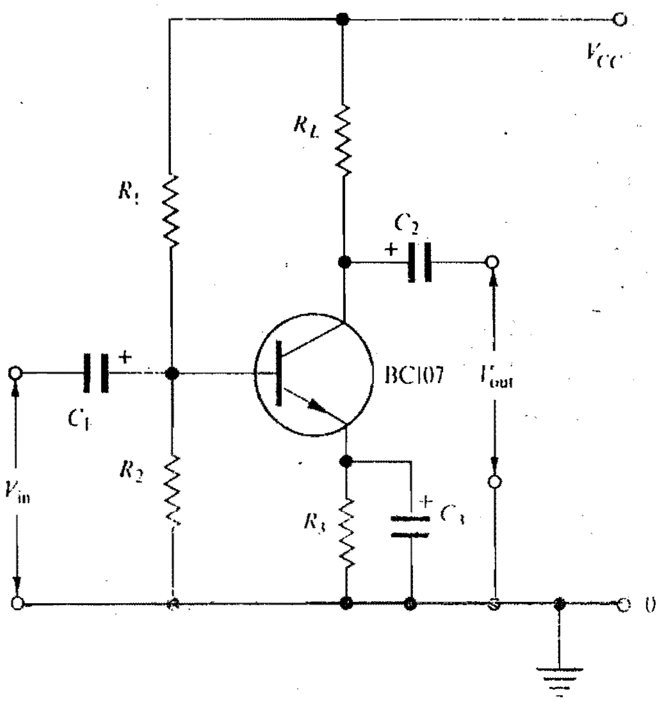

Fig. 1

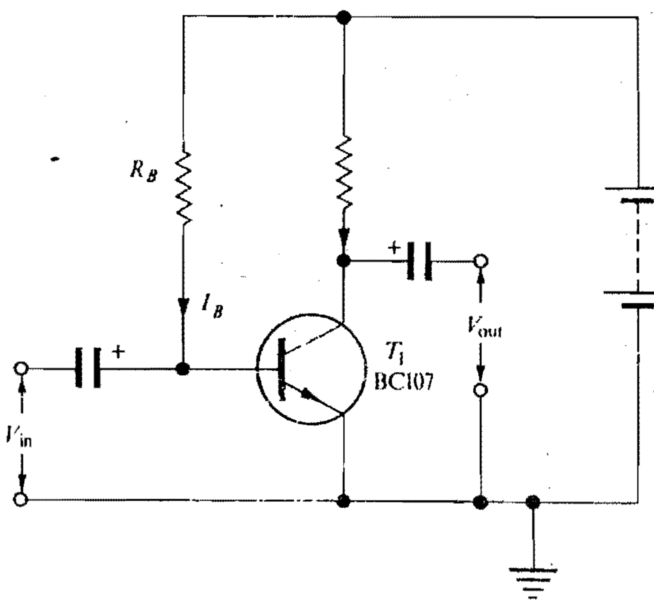

Fig. 2

QUESTION 2

(a) With the aid of diagrams, explain how an n-channel junction gate field effect transistor (jugfet) is fabricated. (7 marks)

(b) Sketch a simple diagram and use it to explain how the jugfet works. Use the drain and mutual characteristics of the transistor to illustrate your point. (8 marks)

(c) The n-channel JFET circuit of Fig. 3 employs one of several methods of self-bias. Assume negligible gate current.

(i) Explain, in detail, why it is called a self-bias circuit. (4 marks)

(ii) Find I_{DQ} and V_{GSQ} when $R_D = 3\ k\Omega$, $R_S = 1\ k\Omega$, $V_{DD} = 15$ V, and $V_{DSQ} = 7$ V. (6 marks)

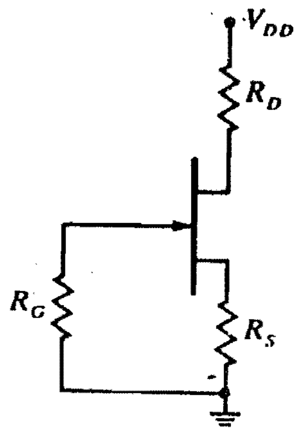

Fig. 3

QUESTION 3

(a) Figure 4 shows a typical voltage regulator circuit. Use this circuit, together with a waveform (ripple from a FWR) which demonstrates the variation of the input voltage, V_i with time, to explain how the circuit works. (10 marks)

(b) The Zener diode in the voltage regulator circuit of Fig. 4 has a constant reverse breakdown voltage, $V_Z = 8.2$ V, for $75 \text{ mA} \leq i_Z \leq 1$ A. If $R_L = 9\ \Omega$, determine a suitable value of R_S so that V_L regulates to 8.2 V while V_i varies by $\pm 10\%$ from its nominal value, 12 V. (6 marks)

(c) A full-wave rectifier with a smoothing capacitor is connected to an a.c. voltage source operating at 60 Hz, as shown in Fig. 5. The load resistor connected across the output terminals of the circuit has a value of 1.5 kΩ. The peak value of the secondary voltage is 18 V whilst the peak-to-peak ripple voltage is 2 V.

(i) Sketch a graph that represents the variation of the output voltage with time in relation to the voltage at the secondary of the transformer. Label it. (4 marks)

(ii) Calculate the capacitance of the smoothing capacitor. (5 marks)

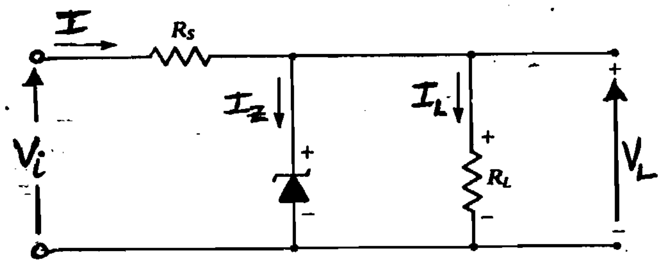

Fig. 4

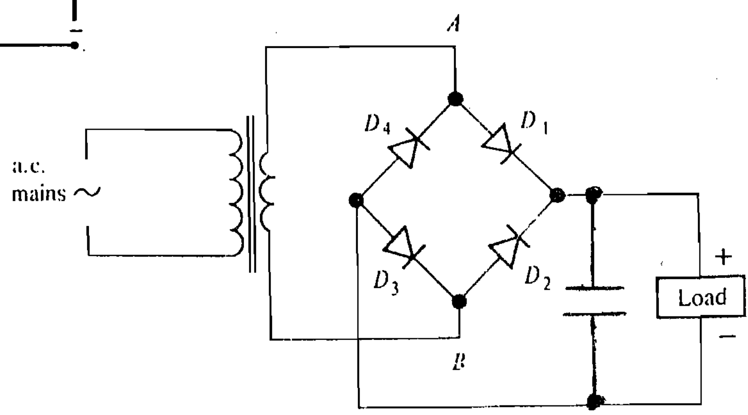

Fig. 5

QUESTION 4

(a) Use appropriate diagrams to explain how a p-n diode works, with reference only to a forward biased diode. (10 marks)

[**Note**: Your explanation should begin with a comment on the non-equilibrium state of the diode, that is, the state where a concentration gradient exists at the junction].

(b) A Si diode has a saturation current $I_o = 10$ nA at T = 300 K.

(i) Find the forward current if the forward voltage is 0.5 V. (3 marks)

(ii) If this diode is rated for maximum current of 5 A, what is the junction temperature at rated current if the forward drop is 0.7 V? (5 marks)

(iii) If the dynamic resistance of the diode $r_d = 100\ \Omega$, what must be the quiescent conditions?

(7 marks)

QUESTION 5

(a) Define the terms drain resistance and mutual conductance of a junction field effect transistor. (4 marks)

(b) Plot the mutual characteristic curve of the transistor in accordance with the equation below. Let $I_{DSS} = 5$ mA and $V_P = -3$ V.

$$I_D = I_{DSS}\,[1 - (V_{GS}/V_P)]^2 \qquad \text{(5 marks)}$$

(c) (i) Calculate the capacitance of the filter capacitor in the rectifier circuit of Fig. 6 when the ripple voltage is approximately 5% of the average value of output voltage. The diode is ideal, $R_L = 1$ kΩ, and $v_s = 90 \sin 377t$ (V). (5 marks)

~~(ii) Find the average voltage across R_L.~~

(d) The Zener diode in the voltage regulator circuit of Fig. 7 has $V_Z = 18.6$ V at a minimum I_Z of 15 mA. If the variable input voltage is 24 ± 3 V and R_L is 2kΩ, what is the maximum value of R required to maintain regulation? (5 marks)

(e) The transistor of Fig. 7 has $\alpha = 0.98$ and a base current of 30μA. Find

(i) β (2 marks)
(ii) I_{CQ} and (2 marks)
(iii) I_{EQ} (2 marks)

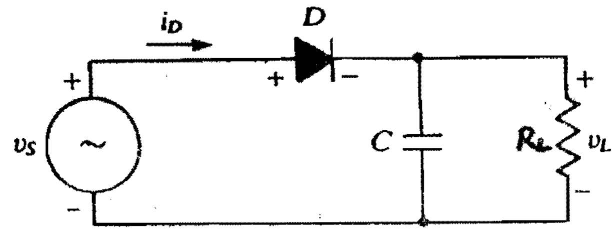

Fig. 6

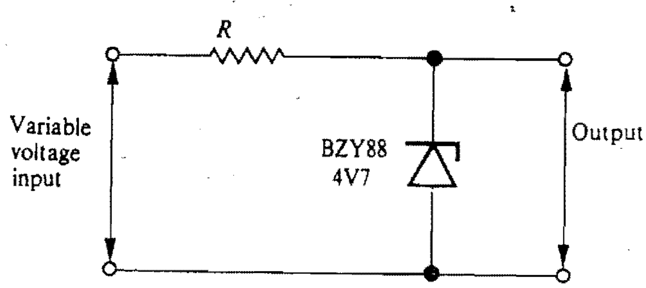

Fig. 7