UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF PHYSICS

MAIN EXAMINATION	2012/13
TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER:	P411
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ANY FOUR OUT OF FIVE QUESTIONS.

EACH QUESTION CARRIES 25 MARKS.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS 7 PAGES INCLUDING THIS PAGE.

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1 (a) (i) The 7's complement of a certain octal number is 5264. Determine the hexadecimal equivalent of that octal number. **[3]**

(ii) Convert the hexadecimal number $2B6D.5AB_{16}$ to its equivatent decimal number. **[3]**

(b) (i) Subract $2B6D.5_{16}$ from $5A6BD.2_{16}$. **[3]**

(ii) Find the equivalent decimal value of the following BCD coded number: 10011101100011_{BCD}. **[2]**

(c) (i) Convert the straight binary number 110011_2 to its Gray code equivalent. **[2]**

(ii) Convert the 2's complement of the quinary number 414_5 into hexadecimal. **[6]**

(d) Consider the two signals simultaneously entering the EX-OR gate in **figure 1** of **Appendix A**. Make a table listing the binary outputs corresponding to the input points labeled a, b,....ℓ. **[6]**

2 (a) Show how you would implement a four-input EX-OR function using two-input EX-OR gates. **[4]**

(b) Write the Boolean expression for the logic diagram in **figure 2** of **Appendix A**. **[5]**

(c) Convert the following Boolean expressions to their **simplest non**-standard SOP forms:

(i) $F = \overline{(A + \bar{B}C + A\bar{B})}$; **[4]**

(ii) $F = \overline{(AB + AC)}$. **[4]**

(d) Minimize the Boolean expression for the logic function
$F(ABCD) = AB\bar{C}D + A\bar{B}\bar{C}\bar{D} + \bar{B}CD + \bar{A}\bar{B} + \bar{A}B\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D}$,
using a Karnaugh map. **[8]**

3 (a) Use the transposition theorem to prove that
$L(M + \bar{N}) + \bar{L}\bar{P}Q = (L + \bar{P}Q)(\bar{L} + M + \bar{N})$. **[3]**

(b) (i) Make the truth table for the sum function, S of a full adder with three inputs A, B and C. Do not include the carry-out function. **[2]**

(ii) Make a truth table for an even parity generator circuit which has three inputs A, B and C with one output P which is the parity bit. **[2]**

(iii) Show how you would implement the functions S and P using a single logic gate. **[6]**

(c) The data sheet of a certain eight-bit A/D converter lists the following specifications: the resolution is eight bits, the full-scale error is 0.02 % of full scale and the full-scale analogue input is +5 V. Determine:

(i) the quantized error (in volts); **[3]**

(ii) the total possible error (in volts). **[3]**

(d) A certain eight-bit D/A converter has a full-scale output of 5 mV and a full-scale error of ±0.25%. Determine the range of expected analogue outputs for a digital input of 10000010. **[6]**

4 (a) **Figure 3,** in **Appendix A,** shows a labeled logic circuit of a four-NAND gate RS flip flop. Copy and complete **Table 1** of **Appendix B** with the various signals at the inputs and output of the clocked RS flip flop. **[4]**

(b) **Figure 4,** of **Appendix A,** shows a negative edge triggered D-type flip flop. The clock pulse and the D-input are shown in a timing waveform diagram to the right of the flip flop. Copy the timing waveform diagram and draw the waveform of the output, Q just below the D-input waveform. Use the same clock pulse timing. **[6]**

(c) **Figure 5,** in **Appendix A,** shows a 4-bit shift register. The clock pulse, clear signal and data input are shown in a timing waveform diagram below the register. Copy the timing waveform diagram and draw the waveforms of the outputs, Q_A, Q_B, Q_C and Q_D just below the data input waveform, using the same clock pulse timing. **[8]**

(d) Identify the logic circuit in **figure 6** of **Appendix A** and explain how it functions. **[7]**

5 (a) RAM chips are available in the memory capacities ranging from 2 kB to 32 MB; here, the terms 'kilo' (k) and 'mega' (M) are approximations that do not exactly represent 10^3 and 10^6 bytes of actual memory respectively. How many bytes of actual memory do these terms represent? **[2]**

(b) A certain ROM is capable of sorting 16 kB of data. If the internal architecture of the ROM uses a square matrix of registers, determine:

(i) the number of registers in each row and column; **[5]**

(ii) the total number of address inputs. **[5]**

(c) It is desired to design a microcontroller-based periodic signal generator with minimum and maximum time period specifications of 125 ns and 100 ms. What should the system clock frequency be? **[5]**

(d) A certain microcontroller has an on-chip 16-bit counter/timer system. It is used to measure the width of an input pulse. The microcontroller has been programmed to measure the time of occurrence of rising and falling edges of an input pulse on a certain I/O pin. If the microcontroller uses an 8 MHz clock and the count values observed at the time of occurrence of rising and falling edges of the input pulse are 001F and 00F1 (in hex), determine the pulse width as measured by the microcontroller. **[8]**

APPENDIX A – DIAGRAMS

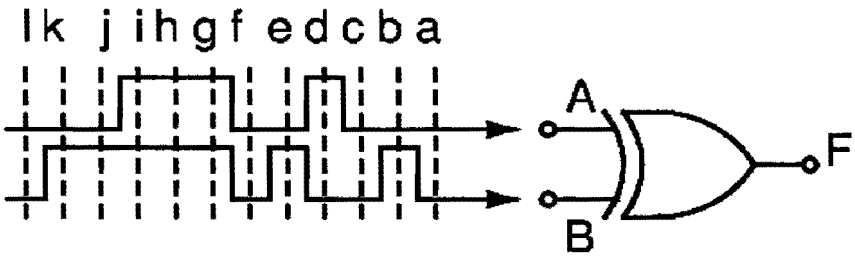

Figure 1

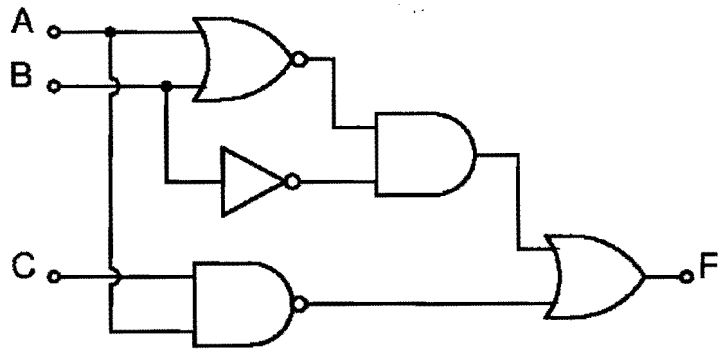

Figure 2

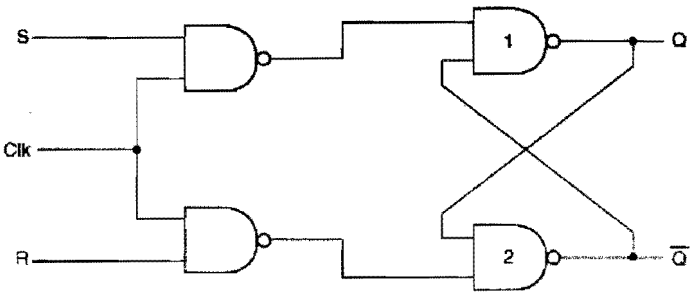

Figure 3

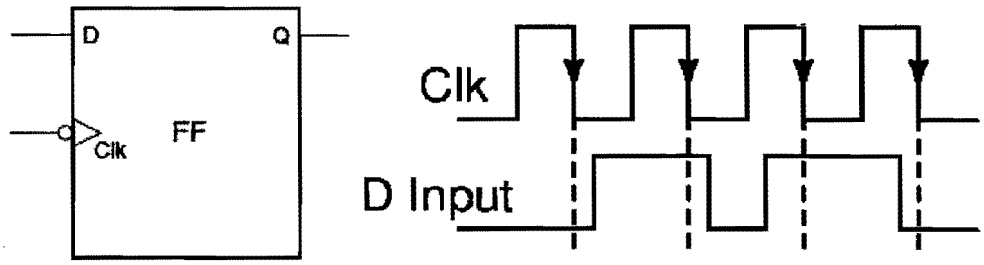

Figure 4

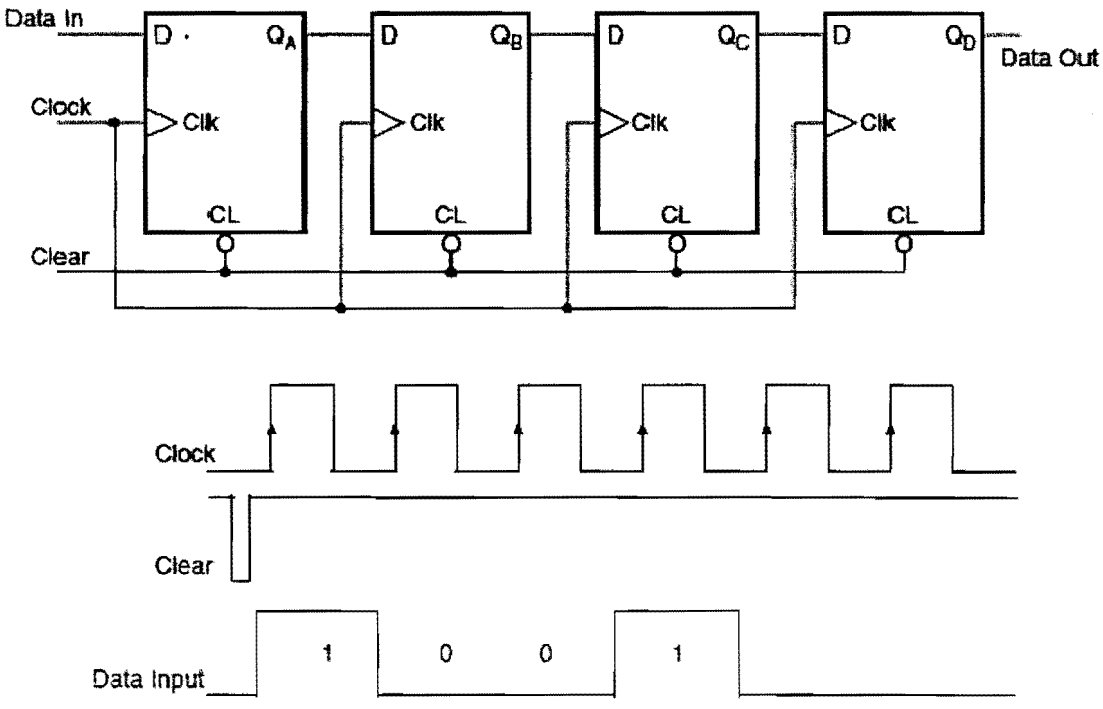

Figure 5

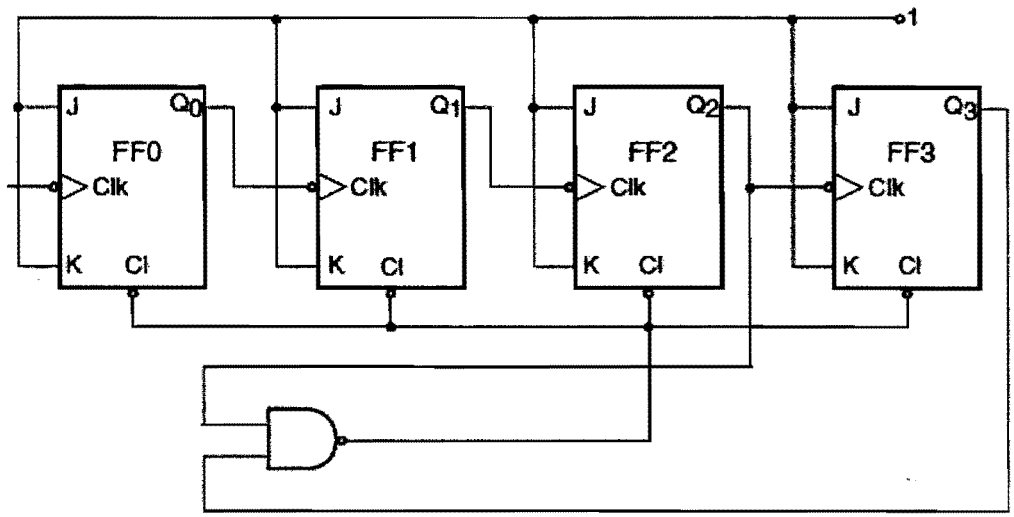

Figure 6

APPENDIX B – TABLE

Table 1

Inputs		Output before the clock pulse	Output after the clock pulse
S	*R*	*Q*	*Q*
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

END OF P411 EXAMINATION