UNIVERSITY OF SWAZILAND

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FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF PHYSICS

SUPPLEMENTARY EXAMINATION	2013/14
TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER:	P411
TIME ALLOWED:	3 HOURS

INSTRUCTIONS:

ANSWER ANY FOUR OUT OF FIVE QUESTIONS.

EACH QUESTION CARRIES 25 MARKS.

MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS 6 PAGES INCLUDING THIS PAGE.

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1 (a) Determine the hexadecimal equivalent of 82.25_{10}. **[4]**

(b) Find the binary equivalent of $17E.F6_{16}$. **[3]**

(c) Find the octal equivalent of $2F.C4_{16}$. **[3]**

(d) Subtract $(-14)_{10}$ from $(-24)_{10}$, using the 2's complement representation. **[5]**

(e) Subtract $29.A_{16}$ from $4F.B_{16}$, using the 2's complement arithmetic. **[5]**

(f) Subtract 77_8 from 12_8, using the 8's complement arithmetic. **[5]**

2 (a) Show two possible arrangements of the hardware-implementing of a four-input OR gate, using two-input OR gates only. **[4]**

(b) The truth table represented in **Table 1 of Appendix B** gives the output F, for inputs A and B. What logic gate would perform this operation? Draw a symbol for this gate. **[3]**

(c) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate,

$$F = A \oplus B = A\bar{B} + B\bar{A}$$

in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. **[7]**

(d) Use maxterms (not minterms) and a Karnaugh map to convert the Boolean expression,

$$y = C + \bar{A}B + A\bar{B}$$

into a canonical POS form. **[7]**

(e) Write the simplified Boolean expression $F(A,B,C,D)$ for the Karnaugh map shown in **Figure 1 of Appendix A**. **[4]**

3 (a) Use AND, OR and NOT gates to construct a circuit that carries out the following logic function:

$$F = \overline{(A\bar{B}C + \overline{A}\overline{B})} + AC.$$ **[6]**

(b) Use the transposition theorem to prove that,

$$[A\bar{B} + \bar{C} + \bar{D}][D + (E + \bar{F})G] = D(A.\bar{B} + \bar{C}) + \bar{D}G(E + \bar{F}).$$ **[5]**

(c) The logic diagram in **Figure 2 of Appendix A** performs the function of a very

common arithmetic building block. Identify the logic function. **[6]** 175

(d) Make a truth table and design a four-line to two-line priority encoder with active HIGH inputs and outputs. Priority is assigned to the higher-order data input line. **[8]**

4 (a) **Figure 3,** in **Appendix A,** shows the internal logic circuit diagram of one of the four *D* latches of a four-bit *D* latch in the 7475 IC.

(i) Give an argument to prove that the *Q* output will track the *D* input only when the ENABLE input is HIGH. **[3]**

(ii) Also, prove that during the time the ENABLE input is LOW the *Q* output holds the value it had just before it went LOW. **[6]**

(b) It is desired to design a binary ripple counter of the type shown in **Figure 4** of **Appendix A** that is capable of counting the number of items passing on a conveyor belt. Each time an item passes a given point, a pulse is generated that can be used as a clock input. If the maximum number of items to be counted is 6000, determine the number of flip-flops required. **[8]**

(c) Determine the number of flip-flops required to construct a MOD-10:

(i) Ring counter; **[4]**

(ii) Johnson counter. **[4]**

Also, write the count sequences in the two cases.

5 (a) Determine the resolution of a 12-bit A/D converter having a full-scale analogue input voltage of 5 V. **[5]**

(b) In computer terminology, distinguish between the terms 'memory' and 'storage'. **[2]**

(c) Two 16 MB RAMs are used to build an extended RAM capacity of 32 MB. Show the configuration and how it works. Also, state the address inputs for which the RAMs will be active. The two RAMs have common I/O pins, a WRITE ENABLE input that is active LOW ($\overline{WE}$) and a CHIP SELECTOR input that is active HIGH (CS). **[10]**

(d) Make short notes to describe the functions of the following elements of a microprocessor unit:

(i) Data register (DR); **[2]**

(ii) Address register (AR); **[2]**

(iii) Arithmetic logic unit (ALU); **[2]**

(iv) Stack Pointer (SP). **[2]**

APPENDIX A – DIAGRAMS

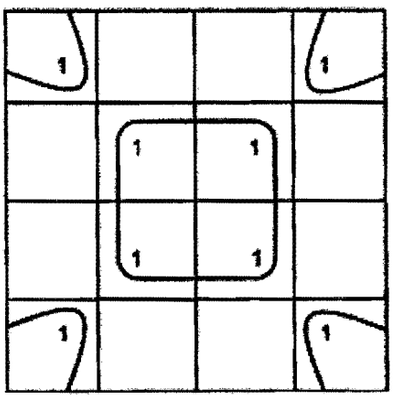


Figure 1

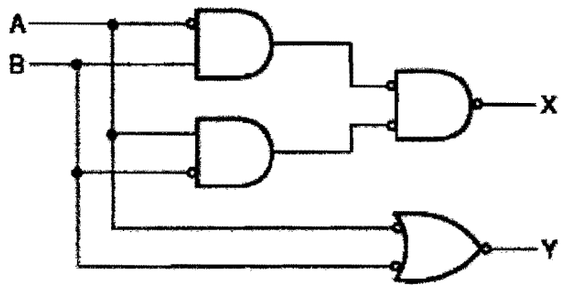


Figure 2

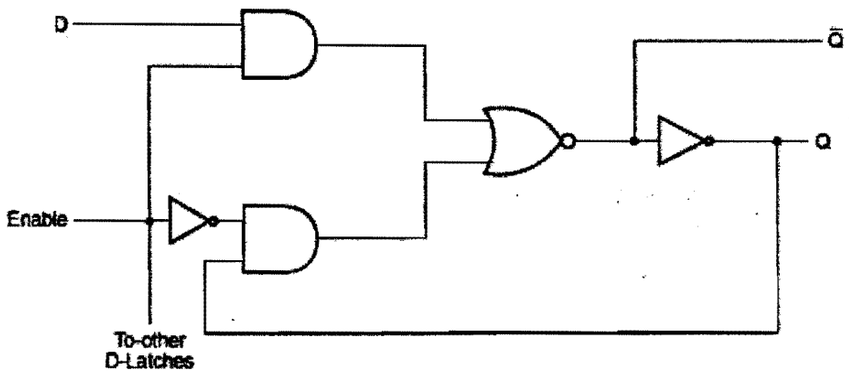
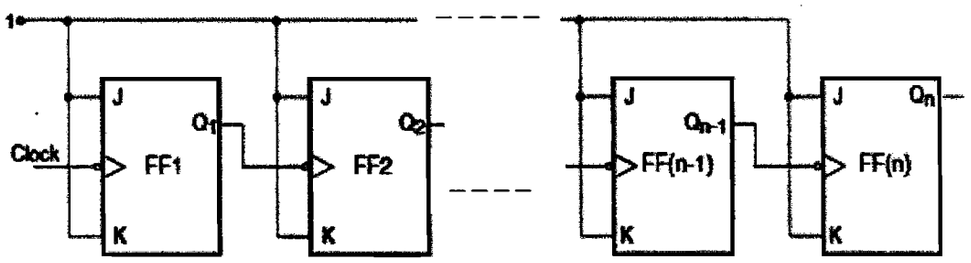


Figure 3



Note: The dashed lines represent an unspecified number of flip-flops connected in the same configuration as FF2 and FF(n-1).

Figure 4

APPENDIX B – TABLE

Table 1

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

END OF P411 SUPPLEMENTARY EXAMINATION