UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF PHYSICS

MAIN EXAMINATION 2015/2016

TITLE OF PAPER	:	ELECTRONICS 1
COURSE NUMBER	:	P311
TIME ALLOWED	:	THREE HOURS
INSTRUCTIONS	:	ANSWER ANY FOUR OUT OF FIVE QUESTIONS
		EACH QUESTION CARRIES 25 MARKS
		MARKS FOR DIFFERENT SECTIONS ARE SHOWN IN THE RIGHT-HAND MARGIN.

THIS PAPER HAS 7 PAGES, INCLUDING THIS PAGE.

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QUESTION 1

(a) (i) Sketch the energy band diagram of silicon that is doped with a Group V element and label it. (4 marks)

(ii) Explain the meaning of the diagram, with reference to majority and minority carriers in the doped silicon lattice. (4 marks)

(b) Consider the following Shockley equation:

$$I = I_S\left[\exp\left(\frac{qV_D}{\eta k_B T}\right) - 1\right],$$

where the symbols have their usual meanings.

Estimate the current, I_D that would flow through a silicon p-n diode at 300 K,

(i) when the forward voltage is + 0.4 V; (4 marks)

(ii) when the reverse voltage is - 5 V. (2 marks)

Assume that the reverse saturation current is 0.05 μA.

(c) (i) Use the Shockley equation to derive an expression for the dynamic resistance, $r = dV/dI$ of a silicon p-n junction diode; (5 marks)

(ii) What will be the dynamic resistance of the diode when the forward voltage is 0.4 V. (3 marks)

(d) Assuming the barrier potential to be 0.6 V, calculate the current flowing in Fig. 1. (3 marks)

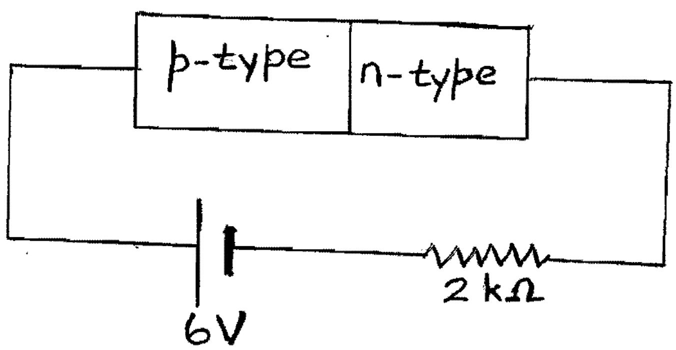

Fig. 1

QUESTION 2

(a) Show that the average output voltage, V_{av} of a half-wave rectifier is approximately one-third of the peak value of the secondary voltage, V_m. (7 marks)

(b) The input transformer of a full-wave rectifier has a turns ratio of 9.58:1. The r.m.s. voltage at the secondary is 24 V. Calculate

(i) the r.m.s. input voltage; (3 marks)

(ii) the peak current flowing in a 200 Ω load; (4 marks)

(iii) the d.c. current in the 200 Ω load. (2 marks)

(c) A Zener diode stabilizing circuit has an input voltage of 18 V and a diode current of 8 mA to give 10 V across a load of 1200 Ω. Calculate

(i) the value of the series resistor; (3 marks)

(ii) the diode current when the load resistance is 1000 Ω. (6 marks)

QUESTION 3

(a) With the aid of a schematic diagram and drain characteristics,

(i) Explain how the depletion layer in the channel of an n-channel JFET varies with the drain-source voltage; (4 marks)

(ii) Explain how the channel resistance varies with this voltage for small voltages; (1 mark)

(iii) What effect stops the variation of the depletion layer at high voltages? (3 marks)

(b) A JFET amplifier has a signal voltage of 1.5 V peak value applied to its input terminals. The drain current then varies by ± 2 mA about its quiescent value. Calculate the transconductance of the JFET. (3 marks)

(c) Calculate the drain load resistance, R_2 required for the circuit of Fig. 2 to give a voltage gain of 20. The JFET used has $g_m = 4 \times 10^{-3}$ S and $r_{ds} = 100$ kΩ. (4 marks)

(d) Fig. 3 shows both the mutual and drain characteristics of an n-channel JFET. If $V_{DD} = 20$ V draw the load line for $R_L = 2000$ Ω on the drain characteristic and select the operating point $V_{GS} = -2$ V. A signal voltage varies V_{GS} between the limits - 1V and - 3 V.

(i) Determine from both sets of characteristics the mutual conductance of the device; (6 marks)

(ii) Calculate the voltage gain (a) from the load line and (b) using the expression $A_v = -g_m R_L$. (4 marks)

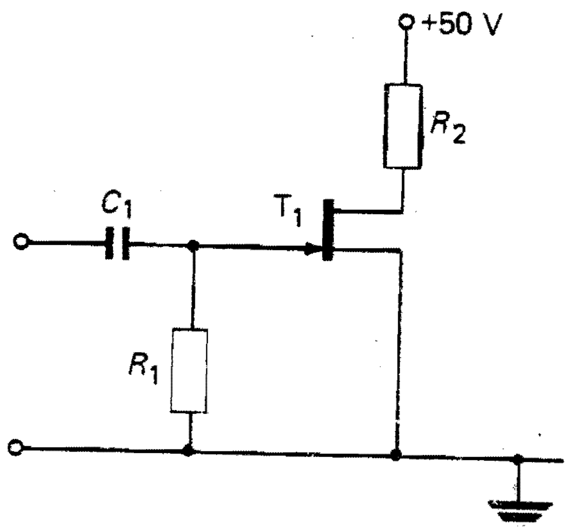

Fig. 2

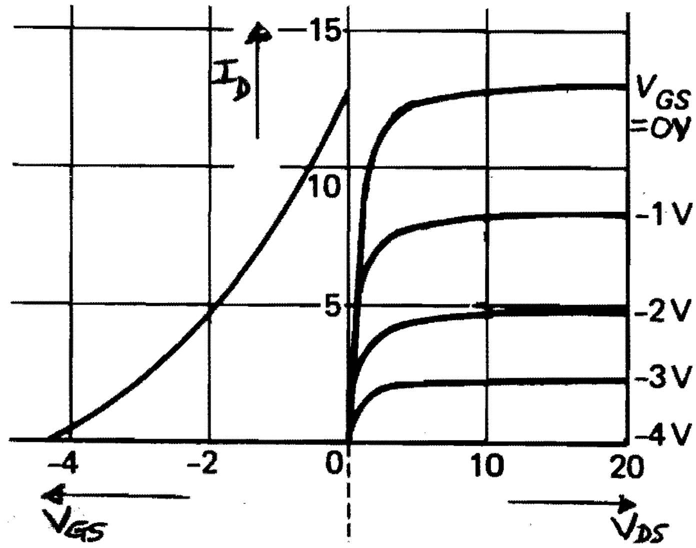

Fig. 3

QUESTION 4

(a) With the aid of data estimated from the output characteristics given in Fig. 4, when V_{CE} is kept constant at 8 V, draw and label the transfer characteristic for the transistor. (4 marks)

(b) The application of a signal voltage of 7.5 mV peak between the base and emitter terminals of an n-p-n transistor causes the emitter current to vary by $\pm$ 0.5 mA about its d.c. value. If the common-base current gain is 0.99,

(i) Calculate the a.c. voltage developed across a 1200 Ω load resistor connected in the collector circuit; (4 marks)

(ii) Calculate the voltage gain of the circuit. (2 marks)

(c) In Fig. 5, V_{CC} = 12 V, I_C = 2mA and V_{BE} = 0.65 V.

(i) If h_{FE} = 100, what is the value of I_B? (2 marks)

(ii) If 1/10th of the supply voltage appears across R_3, calculate R_3; (2 marks)

(iii) If $V_{CE} = V_{CC}/2$ calculate R_L; (4 marks)

(iv) If $I_{R2} = 10I_B$ calculate R_1 and R_2. (7 marks)

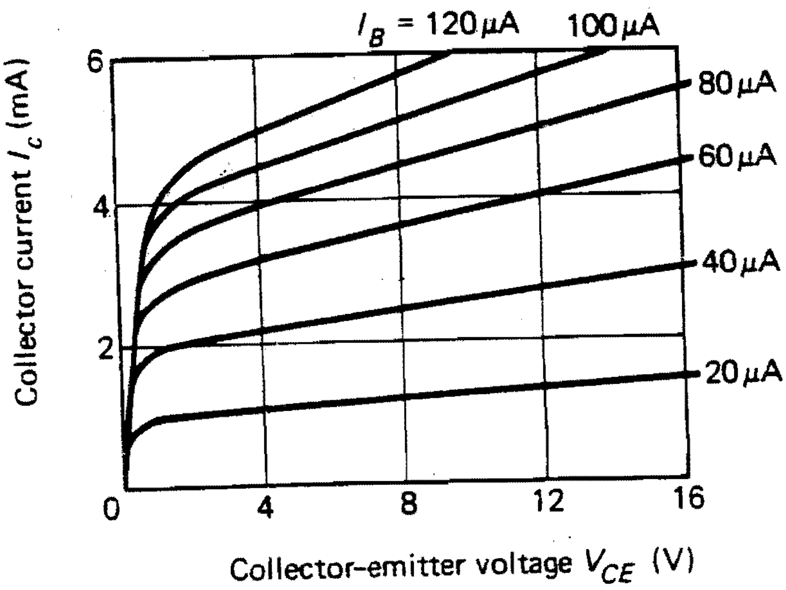

Fig. 4

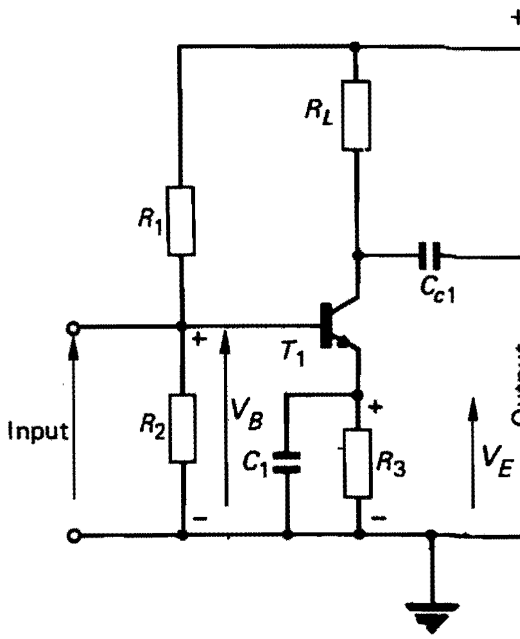

Fig. 5

QUESTION 5

(a) A silicon diode is operated at a junction temperature of 27 °C. For a forward current of 0.15 mA, V_D is found to be 0.4 V. With reference to the following Shockley equation:

$$I = I_S\left[\exp\left(\frac{qV_D}{\eta k_B T}\right) - 1\right]$$

where the symbols have their usual meanings,

(i) Find the reverse saturation current; (3 marks)

(ii) Find the forward current when $V_D = 0.5$ V. (3 marks)

(b) The unfiltered bridge rectifier circuit shown in Fig. 6 is powered by the 120 V_{rms} ac power system, and the turns ratio is $N_p : N_s = 6 : 1$. Determine

(i) The rms secondary voltage; (2 marks)
(ii) The peak secondary voltage; (2 marks)
(iii) The dc load voltage; (2 marks)
(iv) The dc load current if $R_L = 5\ \Omega$. (2 marks)

Neglect any diode and transformer losses.

(c) A Zener diode is advertised as having a breakdown voltage of 20 V with a maximum power dissipation of 400 mW. What is the maximum current that should be allowed through the diode? (2 marks)

(d) The drain-source voltage of a JFET is increased from 6 V to 7 V. The resulting increase in the drain current is 0.1 mA. Calculate the output resistance of the FET. Assume that there is no change in the value of the gate-source voltage. (3 marks)

(e) The circuit shown in Fig. 7 is designed for operation with transistors having a nominal h_{FE} of 100. Calculate the d.c. collector current. If the range of possible h_{FE} values is from 50 to 160, calculate the d.c. collector current flowing if a transistor having the maximum h_{FE} is used. Assume $I_{CEO} = 1\ \mu$A and $V_{BE} = 0.62$ V. (6 marks)

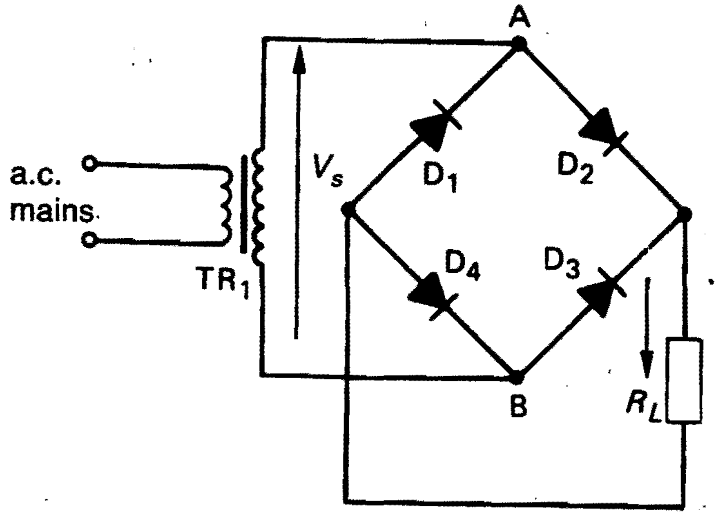

Fig. 6

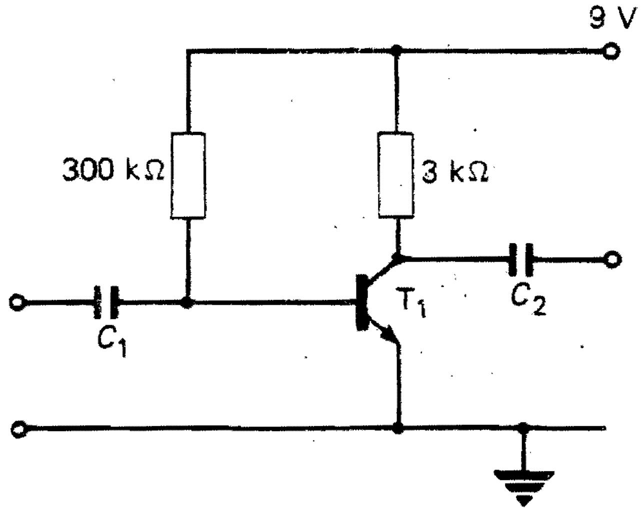

Fig. 7