UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF PHYSICS

MAIN EXAMINATION 2015/16

TITLE OF PAPER:	DIGITAL ELECTRONICS
COURSE NUMBER:	P411
TIME ALLOWED:	3 HOURS
INSTRUCTIONS:	ANSWER ANY FOUR OUT OF FIVE QUESTIONS.
	EACH QUESTION CARRIES 25 MARKS.
	MARKS FOR DIFFERENT SECTIONS ARE SHOWN ENCLOSED IN SQUARE BRACKETS.

THIS PAPER HAS SEVEN (7) PAGES INCLUDING THIS PAGE.

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QUESTION 1

a) Convert the hexadecimal number $2B6D.5AB_{16}$ to its equivalent decimal number. [4]

b) Find the equivalent octal number for the BCD coded number 101011100101_{BCD}. [3]

c) Subtract $(1110.011)_2$ from $(11011.11)_2$ using basic rules of binary subtraction. [4]

d) i) Find the decimal equivalent of the following binary number expressed in the 2's complement format: 00001110_2 [4]

ii) Two possible binary representations of $(-1)_{10}$ are $(10000001)_2$ and $(11111111)_2$. One of them belongs to the sign-bit magnitude format and the other to the 2's complement format. Identify, which is which. [4]

e) Consider the two signals simultaneously entering the XOR gate in Figure 1. Make a table listing the binary outputs corresponding to the input points labelled *a, b,....l* [6]

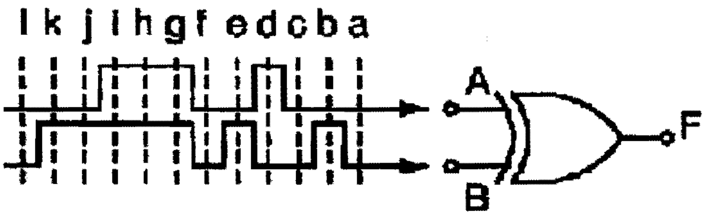


Figure 1

QUESTION 2

a) Draw logic implementation of an inverter using (i) two-input NAND, (ii) two-input NOR, (iii) two-input EX-OR and (iv) two-input EX-NOR. [6]

b) Explain what a 'wired-AND' is, using an example. [4]

c) State the De Morgan's Theorem. [4]

d) Simplify the following expressions using Boolean algebra:

i) $F = (X + \bar{Y} + \bar{X} \cdot Y) \cdot \bar{Z}$ [3]

ii) $F = \bar{X} \cdot Y \cdot (X + \bar{Y} + \bar{X} \cdot Y)(X + \bar{Y})$ [3]

e) Convert the following logical expression into canonical POS or maxterm form:

$F = (A + B)(A + C)(B + C)$ [5]

QUESTION 3

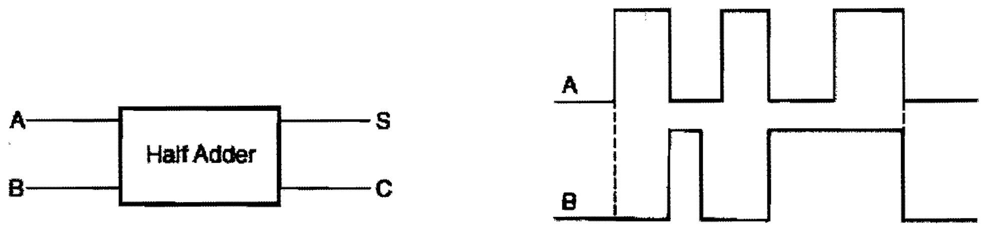
a) Map the function having four variables in a K-map and give the simplified Boolean expression. The function is $F(A,B,C,D) = \Sigma\, m(2,6,10,14)$. [7]

b) Using the Karnaugh Map, simplify the Boolean function given by

$$F(A,B,C) = (A + B + C)(\bar{A} + B + \bar{C})(A + \bar{B} + C)$$

for the don't care condition expressed as $(\bar{A} + \bar{B})(\bar{A} + B + C)$. [6]

c) For the half-adder circuit of Figure 2(a), the inputs applied at A and B are as shown in Figure 2(b). Plot the corresponding SUM and CARRY outputs on the same scale. [4]



(a) (b)

Figure 2

d) Write down Boolean expressions representing the SUM and CARRY outputs in terms of three input binary variables to be added. Design a suitable combinational circuit to hardware-implement the design using NAND gates only. [8]

QUESTION 4

a) How do you characterize or define a combinational circuit? How does it differ from a sequential circuit? Give two examples each of combinational and sequential logic devices. [6]

b) Design and draw up the truth table for a four-line to two-line priority encoder with active HIGH inputs and outputs, with priority assigned to the higher-order data input line. [7]

c) Figure 3 illustrates a clocked RS flip-flop pulse-train with the set (S) and reset (R) inputs drawn above and below the pulse-train, respectively. For each of the eight clock pulses (a to h), list the binary output Q of the flip-flop. [4]

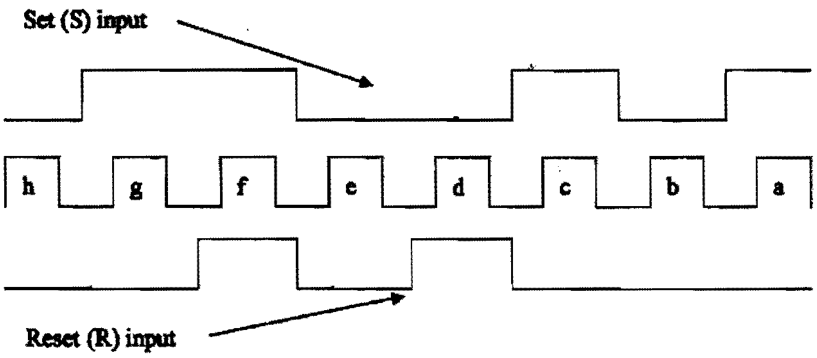


Figure 3

c) For a logic circuit of a four-NAND gate JK flip flop as in Figure 4. Copy and complete Table1 with the various signals at the inputs and outputs of the clocked JK flip flop. [8]

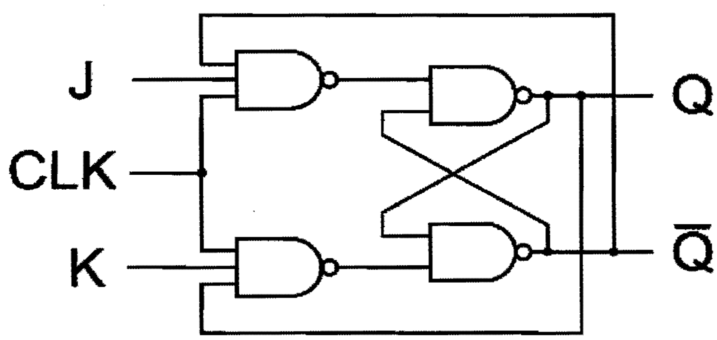


Figure 4

Inputs		Outputs before the clock pulse		Outputs after the clock pulse	
J	K	Q	$\bar{Q}$	Q	$\bar{Q}$
0	0	0	1		
0	0	1	0		
0	1	0	1		
0	1	1	0		
1	0	0	1		
1	0	1	0		
1	1	0	1		
1	1	1	0		

Table 1

QUESTION 5

a) Determine the number of flip-flops required to construct a MOD-10:

(i) Ring counter; [4]

(ii) Johnson counter. [4]

Also write the count sequences in the two cases.

b) Give two uses of shift registers. [3]

c) Determine the resolution of a 12-bit A/D converter having a full-scale analogue input voltage of 5V. [6]

d) Describe the functions of the following elements of a microprocessor unit:

(i) Data register (DR); [2]

(ii) Address register (AR); [2]

(iii) Arithmetic logic unit (ALU); [2]

(iv) Stack Pointer (SP). [2]

END OF P411 MAIN EXAMINATION