UNIVERSITY OF ESWATINI
FACULTY OF SCIENCE AND ENGINEERING
DEPARTMENT OF PHYSICS

MAIN EXAMINATION, DECEMBER 2019

TITLE OF PAPER : DIGITAL ELECTRONICS 1

COURSE NUMBER : PHY 411

TIME ALLOWED : THREE HOURS

INSTRUCTIONS : Answer **FOUR (4)** questions only.

: Each question carries **25 Marks**

: Marks for different sections are shown in far right margin.

THIS PAPER HAS 5 PAGES, INCLUDING THIS ONE.

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1. (a) i. Find the decimal equivalent of the number 11100.01_2. [2]

ii. Convert 34.75_{10} to its binary equivalent. [2]

(b) i. Find the decimal equivalent of the number $EBA.C_{16}$. [2]

ii. Convert 204.125_{10} to its corresponding hexadecimal number. [2]

(c) i. Convert the hexadecimal number $1F.C_{16}$ to its binary equivalent. [3]

ii. Convert the binary number 10100111.111011 to its hexadecimal equivalent. [3]

(d) i. If the number 01001001 is in BCD, convert it to straight binary. [3]

ii. Convert the straight binary number 1001_2 to its Gray code equivalent. [2]

(e) Subtract -23 from -53 using 2's complement binary numbers. Show each step of your working clearly. [6]

2. (a) i. Write the Boolean expression for the AND-OR logic diagram in figure 1. [2]

ii. Make the truth table for the logic diagram in figure 1. [8]

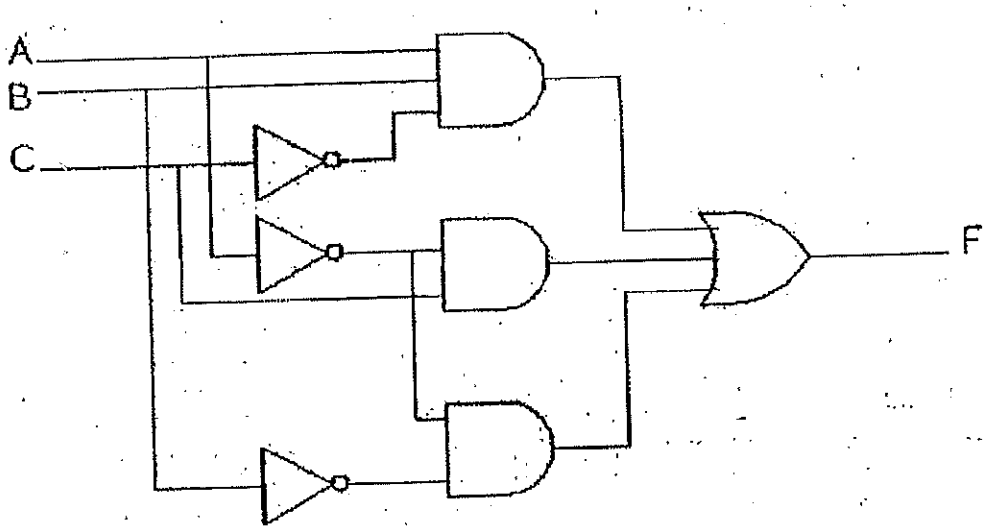


Figure 1:

(b) Draw a logic diagram for the Boolean expression $F = \bar{A}\bar{B} + AB$ using only 2-input NAND gates. [5]

(c) Convert the following Boolean expressions to their standard SOP or minterm forms:

i. $F = \overline{(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})}$; [4]

ii. $F = \overline{(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + \bar{C}) + (CB\bar{A})}$. [6]

3. (a) Show two possible arrangements of the hardware-implementing of a four-input OR gate, using two-input OR gates only. [4]

(b) The truth table represented in Figure 2 below gives the output of F, for inputs A and B. What logic gate would perform this operation? Draw a symbol for this gate. [3]

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

Figure 2:

(c) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate,

$$F = A \bigoplus B = A\bar{B} + B\bar{A}$$

in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. [7]

(d) Use AND, OR and NOT gates to construct a circuit that carries out the following function: [5]

$$F = \overline{(A\bar{B}C + \overline{AB})} + AC$$

(e) The logic diagram in Figure 3 performs the function of a very common arithmetic building block. Identify the logic function. [6]

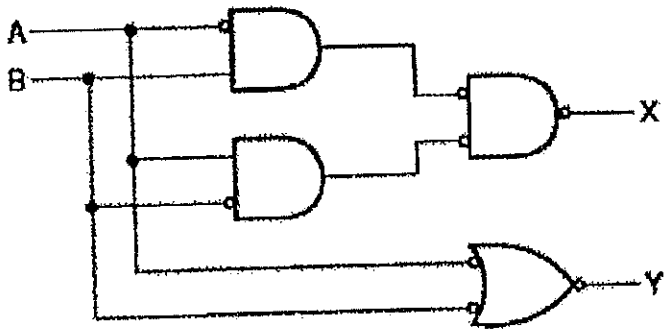


Figure 3:

4. (a) State the procedures of logic function minimization using a K-map. [2]

(b) Given a logic function of three variables, $F(A, B, C) = \sum m(2, 4, 7) + \sum d(1, 3, 6)$. Map the function in a K-map and give the simplified Boolean expressions of F. [6]

(c) Using the Karnaugh Map, simplify the Boolean function given by

$$F(A, B, C) = (A + B + C)(\overline{A} + B + \overline{C})(A + \overline{B} + C)$$

and the don't care condition expressed as $(\overline{A} + \overline{B})(\overline{A} + B + C)$. [6]

(d) Use maxterms (not minterms) and a Karnaugh map to convert the Boolean expression,

$$y = C + A\overline{B} + B\overline{A}$$

into a canonical POS form. [7]

(e) Write the simplified Boolean expression $F(A, B, C)$ for the truth table shown below and draw its logic circuit. [4]

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

5. (a) Differentiate between a half and full Adder. [2]

(b) The truth table for a full subtractor is given in Figure 4.

i. Determine the Boolean expressions representing Difference and Bout. [3]

ii. Draw the logic diagram of a full subtractor using AND, XOR, OR and NOT gates. [3]

Figure 4:

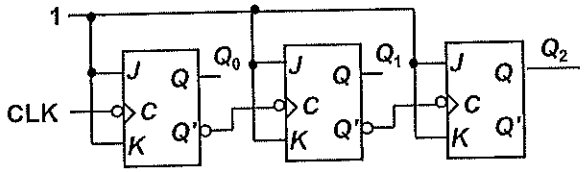
INPUTS			OUTPUTS	
A	B	BIN	BOUT	Difference
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(c) Draw a well labelled excitation table of a negative-edged JK Flip-flop. [2]

(d) Sketch and label a timing diagram of the JK Flip-flop mentioned above. [2]

(e) Write the logic function for the output Q_{n+1} of the flip-flop. [1]

(f) A 3-bit binary (MOD-8) down counter is shown in the Figure below.



Draw the timing diagram and the state sequence of the counter. [6]

(g) Give any six different ways of basic data movement in a 4-bit shift register. [6]

END